Summary of Transients (Old and New) Affect Protection Applications

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***Abstract*— This paper examines the impact of power system transients on the application and setting of protective relays. This summary focuses primarily on unusual transients. Although the impacts of many transients are well known, other transients are not as well recognized or as frequently encountered. In this paper, the authors share their experiences with other less widely reported transients that have either required special settings or design of the protection system to mitigate them.**

***Keywords*: power system transients, protective relaying.**

I. Introduction

MANY transients are already well recognized in the field of power system protection. Their effects are mitigated by application or setting of the protection systems including suitable design of the system, increased margins in settings, and suitable time delays to override transient conditions. Changing power system conditions and changing protective relaying technology has resulted in the emergence of new types of transients and new impacts on protection systems. It is the authors' hope that this paper will increase the awareness of other protection engineers and power system analysts of more unusual transients which may require mitigation measures.

This paper summarizes a more complete review of the types of transients and their impacts that can be found in [1].

II. Background

Short circuits themselves are transients. The power system is not viable with a steady state short circuit applied. Notwithstanding the transient nature of short circuits, protection engineers often model fault conditions as steady state conditions for the purposes of calculating quantities that a relay should measure to discriminate between faults and acceptable (normal) conditions.

The challenge for protection then is to ignore the transients that are present, though not modeled in conventional short circuit studies, while paying full attention to the transient fundamental frequency components that are modelled in the short circuit studies.

Transients can be classified into two broad categories from the protection engineers' point of view – those that originate in the primary power system, and those that are spurious, produced by the instrument transformers and/or secondary wiring connected to the relays. This paper designates the former as "primary" transients, and the latter as "secondary" transients. Within those two categories, infamous and insidious transients are also classified in this paper..

III. Infamous Primary transients

This section is classified as infamous because the transients listed here are well known and widely reported in the literature. They are mentioned here only for completeness and to provide references for the interested reader. The following primary transients are considered to be "infamous" and will not be described in this summary paper.

- Transient offset of fault current [2],[3]
- Harmonics [4]-[6]
- High frequency travelling waves caused by faults
- Low frequency transients caused by series capacitors [7]
- Low frequency power swings (impact on distance relays)
- Frequency excursions causing improper performance of memory polarizing signals[8]
- Transformer and shunt reactor inrush currents[9]
- Shunt capacitor inrush and outrush currents [10]
- Ferroresonance [11]
- Fundamental frequency unbalances resulting from single phase tripping and reclosing [12]

IV. Insidious Primary transients

The following transients are called insidious because they (or their impact on protection) are not as widely recognized as the infamous ones listed in Section III above. Insidious transients are described in more detail than the infamous transients because they are either not reported at all (with respect to protection system impacts), or are reported less widely than the infamous ones.

A. Transmission line ringdown voltages and currents (impact on shunt reactor protection, and impact on distance relay polarizing voltages)

De-energization of a shunt reactor compensated transmission line will result in the shunt reactor inductance oscillating against the line shunt capacitance. Due to the three phases oscillating at slightly different frequencies and inter-phase energy transfer via phase to phase capacitance and

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Paper submitted to the International Conference on Power Systems Transients (IPST2015) in Cavtat, Croatia June 15-18, 2015

neutral reactors, the currents in each phase are not constant, but follow a low frequency envelope. Figure 1 shows the ringdown voltages (VA, VB and VC) and currents (IA, IB, IC) from a shunt reactor connected to a 230 kV circuit which was a mix of overhead line and undersea cable. The ratio of highest peak phase current to the pre-fault peak current is approximately 2.8.

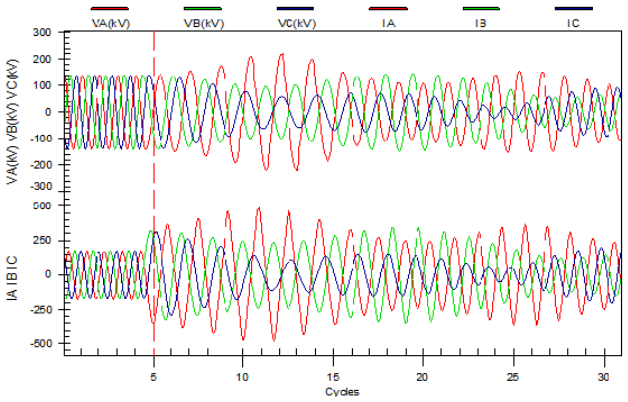

Figure 1 Ringdown voltage and current in shunt reactor after line deenergization.

The maximum phase current in the shunt reactor can be calculated as $I_{RMS} = V_{L-L} \cdot \sqrt{\frac{C}{L}}$ (1),

Where I_{RMS} is the rms phase current, V_{L-L} is the line to line voltage (V), C is the line capacitance per phase (F) and L is the per phase reactor inductance (H)

This current exceeds normal rated reactor current for undercompensated lines. This increased reactor current must be taken into account when calculating phase overcurrent settings for the reactor protection. In addition, if the ringdown frequency of the line is outside of the frequency tracking range of the relay, errors caused by improper filtering can result in transient misoperation of overcurrent elements even if the actual current is below the element pickup. In cases where this is a consideration, a minor time delay on overcurrent element pickup can help prevent transient misoperation, as the error in the calculated current magnitude tends to oscillate about zero.

These low frequency voltage oscillations can also cause problems for memory polarized mho distance elements, as the memory voltage can become corrupted during the interval while the line is ringing, with subsequent “surprises” from the mho elements when the line is reclosed at the first end and line charging current starts to flow again. Each relay manufacturer will deal with this problem internal to the relay in their own way. If the manufacturer has not been successful in avoiding undesirable behaviour, one recourse to the protection engineer is to temporarily block or delay tripping of the mho elements during line re-energization. The switch on to fault logic will still provide protection during re-energization even if the mho elements are temporarily blocked.

It should be noted that if a manufacturer chooses to disable memory polarizing whenever the line terminal is open, it may be necessary to use switch on to fault protection even when using bus side VTs. A current based or offset distance based switch on to fault protection may always be required to protect against switching on to a close-in three phase fault. This is contrary to normal expectations that when bus side VTs are used, memory polarizing will be available for switch on to fault protection of directional distance elements.

B. Fundamental frequency unbalance currents and voltages caused by controlled closing or opening or staggered closing of circuit breakers

As noted previously in this paper, the unbalances resulting from open phase conditions due to single phase tripping are well recognized. However an increasing number of applications of circuit breakers include controlled closing, or point on wave closing to minimize switching transients. Some applications of controlled opening are also applied (particularly in switching of shunt reactors). Controlled closing means that breaker pole discrepancies may last significantly longer than the 4 ms or so that is typically expected for a three pole switched breaker. In some cases, the pole discrepancy may last for several power frequency cycles.

Some means of mitigating the impact of fundamental frequency unbalances due to controlled opening or closing include:

1. Extending the time delay of sensitive unbalance overcurrent functions that might undesirably respond to the short duration unbalance.
2. Disabling the controlled switching when it is not needed. For instance, when controlled closing is applied on a transmission line terminal, only the lead terminal needs to have controlled closing. When the lead terminal closes with pole discrepancy, only low magnitude line charging currents will flow; so unbalance current will be small. When the follow terminal closes, if controlled closing is used (even though not necessary) unbalance currents will be much larger, due to load flow when the follow terminal is closed.

In some cases, controlled switching may not perform as desired. Protective relay disturbance records can help identify such cases. Figure 2 shows the phase voltages (VA, VB, and VC) and currents (IA, IB, and IC) and residual current (IRes) during de-energization of a shunt reactor. In the case of Figure 2, the controlled opening did not operate as expected on all three phases, and the unsuccessful attempt to interrupt A phase current can be seen with the associated restrike showing as a dip and recovery in A phase voltage. The extended neutral current due to slow interruption of A phase load current can be seen. Figure 3 shows the instrument transformer secondary currents and voltages during properly controlled switching.

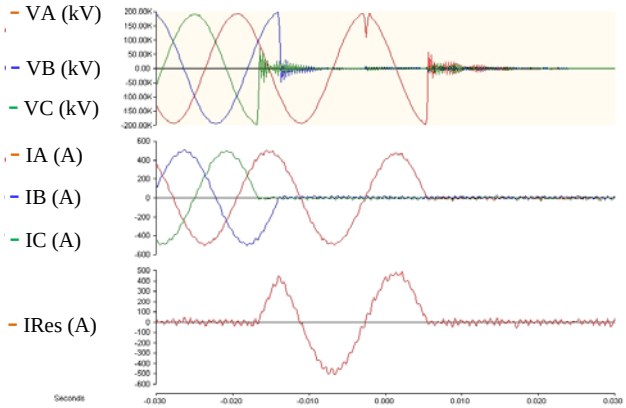

Figure 2 Failure of controlled opening of shunt reactor breaker

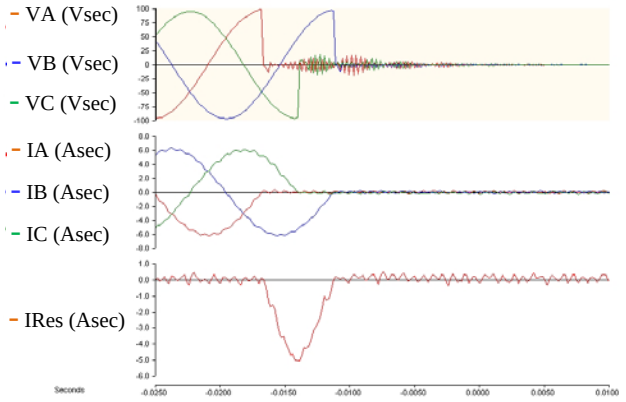

Figure 3 Controlled opening of shunt reactor breaker

C. Gapped surge arrestor conduction due to lightning

Early types of surge arresters included gaps that flashed over to prevent transient overvoltages. Current flows through the flashed gap until the first natural current zero is reached. This flow of so called “follow current” could cause very fast protection to detect a fault and trip undesirably. BC Hydro has experienced some undesirable trips of high speed bus differential protection due to gapped surge arresters in the differential zone.

Figure 4 shows a single line diagram of a BC Hydro station with gapped surge arresters on the high voltage bushing of a transformer. These arresters were inside the differential protection zone of two high impedance bus differential relays 87B and 87BS. The 87B and 87BS relays were of different manufacture. Digital fault recorders (DFR) are connected to measure the currents in each of the transmission line terminals 5L92 and 5L94.

Figure 5 shows a DFR recording of an undesirable trip of the bus protection during a lightning storm. The top three traces are VA, VB and VC of the voltages at the 5L94 line capacitor voltage transformer. The distortion of B Phase voltage at about 4.5 cycles into the recording can be seen. It is apparent that the lightning strike was at the instant VB was near a peak value. The flow of neutral current as soon as the surge arrester started to conduct can be seen in the fourth analogue trace from the top. The conduction stops at the first

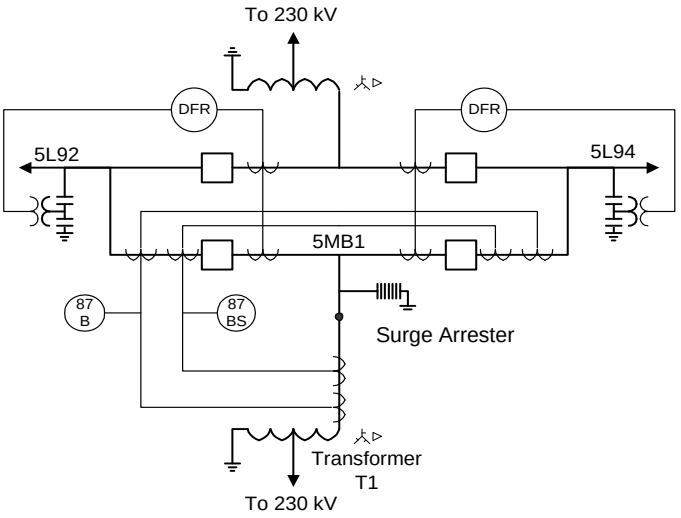

Figure 4 Single line diagram of station with gapped surge arresters

natural current zero. The operation of the high speed bus differential relay due to the apparent internal fault can be seen.

Note that in this instance and in several other instances, the second bus differential relay, made by a different manufacturer, did not operate even though it was set similarly to the one that did operate. The relay that did not operate was not quite as fast as the one that did. The solution applied in this case was to replace the relay that operated undesirably with the same type that was stable during the arrester conduction.

Figure 5 also shows some other digital events on 5L94 primary protection (PY PN.) at the same time as the surge arrester conduction. These events include operation of the sensitive forward looking directional ground overcurrent element in circuit 5L94, and received permissive trip. These events record a near misoperation of the line protection as the forward looking fault detector reset one or two milliseconds before the permissive trip signal was received from the remote terminal. No action was taken with respect to the near miss.

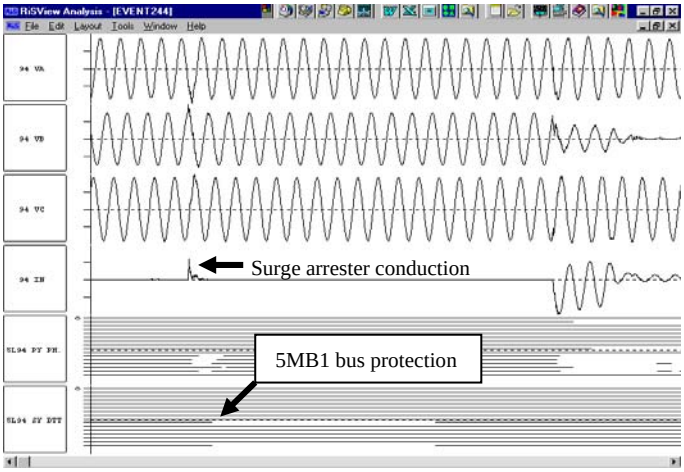

Figure 5 DFR Record of undesirable bus protection operation

The 5L94 line protection was working satisfactorily as can be seen from a correct single phase trip about 4 cycles before the end of the trace, when a second lightning strike caused a real short circuit on B phase and a desirable B Phase trip of circuit 5L94.

D. Low frequency due to series capacitors may affect negative sequence elements

Figure 6 shows a fault record where a healthy series compensated line undesirably tripped, due to sub-synchronous resonance-induced transients after the successful tripping of the adjacent line on a phase to phase fault. The top set of three traces are the (filtered) three phase currents. The next set of three traces are the magnitudes of the three phase currents. The third set of two traces are the magnitudes of the positive and negative sequence components of the three phase currents. All current units are amps rms. Digital events are in the following order.

- IN4 indicates received permissive trip from the remote terminal.
- 67Q2 indicates operation of the forward looking directional negative sequence overcurrent element.
- 67Q2T indicates time out of the security timer for the negative sequence overcurrent element.
- Z3RB indicates operation of the reverse looking blocking function that prevents undesirable tripping during an external fault and for a short time after the external fault is cleared.
- 3PT indicate output of a three phase trip signal to the line breaker.

The undesirable trip was caused by incorrect operation of a sensitive ground fault permissive overreaching transfer trip (POTT) scheme using negative sequence directional and overcurrent fault detectors. Initially, the reverse blocking function (Z3RB) was asserted for the fault on the adjacent line. After the fault on the adjacent line cleared, forward-looking negative-sequence fault detectors picked up at both terminals of the unfaulted line. Pickup of the remote forward fault detector is illustrated by the permissive trip received on IN4 and locally by 67Q2 and 67Q2T. The forward fault detectors remained asserted until shortly after the current reversal guard logic, Z3RB timer, dropped out, 5.5 cycles after the fault was cleared on the adjacent line. At that point, the forward pilot tripping element, coupled with permissive from the remote terminal, allowed a POTT trip.

Analysis of the recordings indicates that a significant resonant current flow with a frequency of around 38 Hz was excited between the B and C phase elements of the power system by the initial fault. When the faulted line opened, all of this resonant current flowed through the healthy line. The relay digital filters attenuate but do not fully reject these sub-synchronous harmonic (or low) frequency components. Since these low frequency components were only in two phases, they consisted of positive- and negative-sequence components similar to an internal phase-to-phase fault. In this case there was enough spectral leakage from sub-harmonic frequency to 60 Hz during signal filtering that the erroneous negative sequence components became large enough to assert the fault detectors. Since the source of sub-synchronous transients was the series capacitor internal to the line and the transients were similar to an internal fault, the directional detectors also got confused and declared a forward direction at both line terminals, leading to the false-trip.

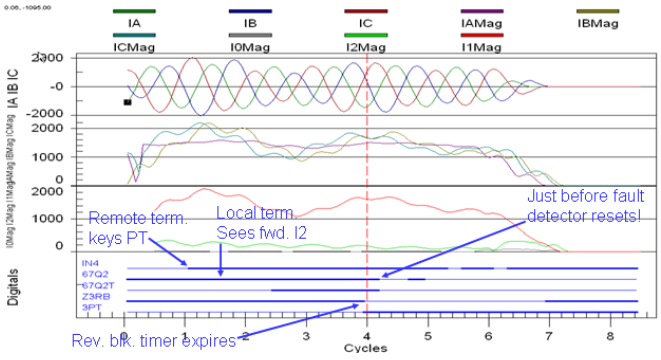

Figure 6 Line protection mis-operation during sub-synchronous resonance

On one hand, the negative-sequence fault detector is well-suited for sensitive ground fault protection of parallel lines due to its immunity to zero-sequence mutual coupling. On the other hand, this incident demonstrates its vulnerability to sub-synchronous resonance transients. Both situations were mitigated by using zero sequence overcurrent fault detection and negative sequence directional element.

E. Extended unbalance from single phase tripping and reclosing

As noted previously in discussion of “infamous” items, unbalances due to single phase tripping are well recognized. However, not so well recognized is the impact of single phase tripping on breaker pole discrepancy timers. In the case of three phase tripping normal discrepancies are less than one cycle in duration, and pole discrepancy timers need only be set marginally longer. However, in the case of single phase tripping, pole discrepancy timers will also be extended to cope with open phase conditions. This means that unbalance overcurrent relays may have to have time delays extended sufficiently to override long pole discrepancy timer settings.

In one case in BC Hydro, a shunt reactor connected to the tertiary winding of a 500 kV auto transformer used negative sequence time overcurrent protection to detect interturn faults. The transformer was adjacent to a line terminal with single phase tripping and reclosing, as shown in Figure 7. Device 50QT in Figure 7 is a negative sequence definite time overcurrent relay.

This protection had been secure for many years even though the transformer was connected to a station where the major supply line had single phase tripping and reclosing applied.

On one occasion however, when breaker 1 was out of service for maintenance, a fault occurred on Line 1 and a

single phase was tripped. Breaker 3 reclosed successfully, but breaker 2 failed to reclose the open pole when commanded to do so. Breaker 2 was normally the second breaker to close in the sequence, (after about 2 seconds). Eventually Breaker 2 pole discrepancy timer opened all three poles correctly and the transformer reactor was disconnected on all three phases.

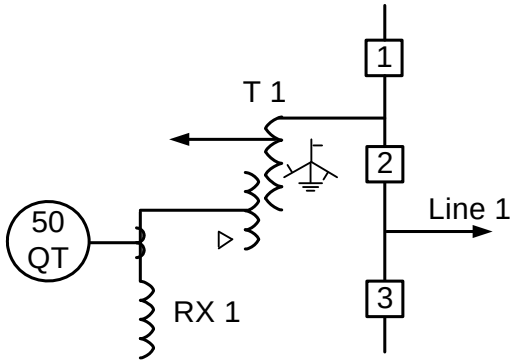

Figure 7 Single phase tripping line and adjacent transformer/reactor

Breaker 2 pole discrepancy timer was set to override a normal open pole period of 2 seconds and was therefore set at 2.5 seconds. Device 50QT was set to override only the normal open phase period of 1 second. It was not set to override the pole discrepancy period of Breaker 2. During the disturbance transformer T1 and reactor RX1 were connected to the 500 kV supply system on only two phases until Breaker 2 pole discrepancy timer expired. The result was that 50QT timed out first, and there was an undesirable lockout trip of the reactor and T1. The mitigation action was to increase the time delay on 50QT.

V. Infamous Secondary Transients

The following list of transients developed in the secondary circuits connected to protection systems are well known in the protection industry, and simply listed here with references for completeness.

- Incorrect differential currents due to unequal current transformer (CT) saturation [13], [14]
- Improper declaration of breaker failure due to DC tail resulting from CT saturation [14]
- Capacitor voltage transformer (CVT) transient inaccuracies [14]
- High frequency/high magnitude secondary voltages [15]
- Spurious signals caused by multiple grounds on voltage transformer and CT secondaries resulting in improper relay performance [16]

VI. Insidious Secondary Transients

A. CT saturation due to long time constants during reactor energization (spurious unbalance currents)

A high X/R ratio (in the range of 500-1000) is required for shunt reactors to minimize their losses. This high X/R ratio results in offset currents with long time constants, in the order of seconds, after reactor energization. Figure 8 shows a time constant of about 2 seconds for the offset current upon energization of a 230 kV shunt reactor.

This very long offset current will saturate current transformers even at low current levels such as normal load. The degree of offset is different between the three phases; so the CT performance will also normally be different between phases and there will be different degrees of saturation (and thus error) in the three CTs. This phenomenon and its

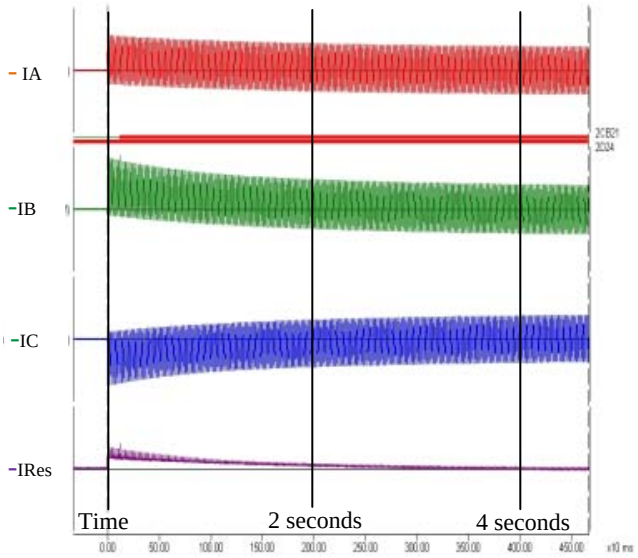

Figure 8 Shunt reactor energization currents

mitigation techniques are completely described in [17]. However, it is mentioned here for completeness and as a refresher. Figure 9 (from [17]) shows how the CT in one phase may saturate more than CTs in the other two phases because of different degrees of offset in the primary currents.

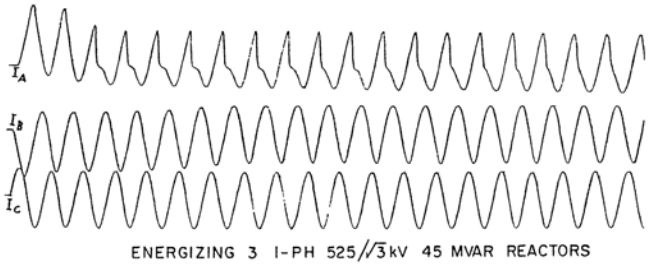

Figure 9 Unequal CT saturation during reactor energization (from [17])

These different degrees of saturation will result in incorrect presence of unbalance currents such as negative sequence or residual during energization. Unbalance overcurrent protection may undesirably operate due to fictitious unbalance current. A mitigation technique that may be used is temporary disabling of sensitive unbalance overcurrent protection during shunt reactor energization (so called inrush tripping suppression). Another technique is to use a neutral CT instead of a residual current of phase CTs to measure zero sequence unbalance current.

If the burden or accuracy class of the CTs at each end of a

winding are different, there could also be undesired operation of differential protection due to unequal saturation of CTs at each end of the reactor. Mitigation methods for this problem include setting differentially connected overcurrent relays higher than load current, or using saturation tolerant differential protection such as high impedance bus differential protection.

Figure 10 (also from [17]) shows the different performance between CTs in a power transformer tertiary and CTs at the neutral end (i.e. CB3 N) of a shunt reactor. It can be seen that the C phase tertiary CT does not saturate significantly in the presence of the transiently offset load current, but the C phase CT on CB3 N does, and a high differential current results.

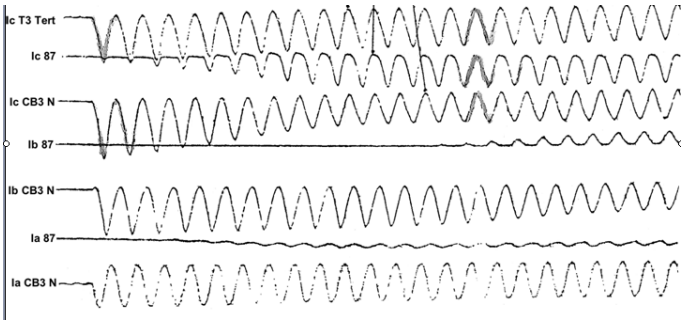

Figure 10 False differential current from unequal CT saturation in the same phase (from [17])

B. DC grounds or ac/dc cross triggering sensitive dc inputs

Although this problem may be classified as “infamous” because it has been well reported (for example in [18]), the increasing application of electronic devices with inputs that can be asserted with low energy levels, has resulted in increased observation of this problem. For this reason the authors have decided to classify this problem as “insidious”. BC Hydro experienced several protection mis-operations from erroneous pick-up of digital inputs of new microprocessor-based relays. These mis-operations were attributed to capacitive discharge and DC voltage transients imposed on high impedance digital inputs.

BC Hydro investigations showed that only a small amount of energy is required to assert sensitive inputs. There are multiple actions that resulted in an inadvertent operation, one of which is a low-impedance ground on the substation (+) DC voltage bus.

Two mitigation strategies to prevent inadvertent relay operation may be considered. First, if the value of secondary control wiring capacitance can be kept as low as possible (for example by avoiding or minimizing the use of surge suppression capacitors on secondary wiring), then the time constant may be such that the voltage will not remain above the relay input pickup level for long enough to be detected. Second, a shunt resistor may be placed across the relay input in order to set up a voltage divider with the leakage resistance of the device connected to the input. With an appropriately sized resistor in the voltage divider, the highest voltage seen across the relay input due to the capacitive transients can be kept below the relay input pickup level.

C. Momentary dc interruptions simulating change of status to inputs

Modern numerical relays are designed to tolerate and even ride through sudden temporary voltage depressions on the dc power supply without undesired effects. However, where the security of a protection system requires assertion of an input signal, the possibility of undesired tripping arises if there is a disturbance on the dc power supply.

Consider for instance the stub line protection function that is sometimes applied as part of a transmission line protection system. This type of protection is sometimes used if the terminal of a transmission line could become separated from the line itself by an open disconnect switch, and if the voltage source for the protection is on the line side of the disconnect switch. The applicable single line diagram and logic diagram are both shown in Figure 11. In Figure 11, Device 50 is an overcurrent protection function, Device 89 is a disconnect switch, Device 89a is an auxiliary switch contact of the disconnect switch (open when the main contacts are open).

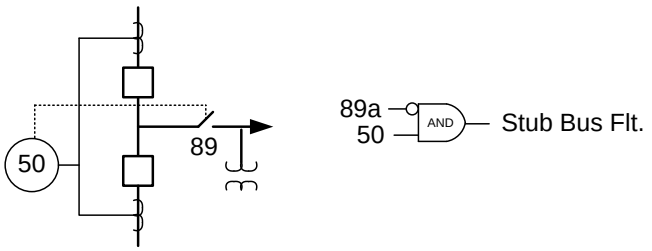

Figure 11 Stub bus protection system

It can be seen from Figure 11 that if the line disconnect switch is open (i.e., auxiliary contact 89a is not asserted) the overcurrent function becomes a simple differentially connected overcurrent system.

If the wetting voltage to the 89a switch is considered, as shown in Figure 12, it can be seen that the power supply may be shared by other protection and control circuits.

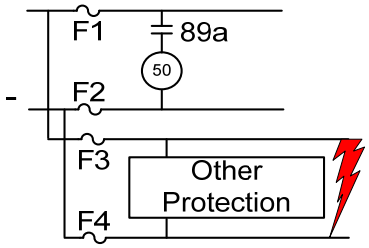

Figure 12 Short circuit on dc power supply.

If there is a short circuit on another circuit as shown, the wetting voltage to Device 50 will be momentarily reduced until such time as the fuse(s) F3 and/or F4 clear the external short circuit. While the wetting voltage is reduced, input 89a is momentarily de-asserted even as the ride through capability of Device 50 allows it to stay in operation. If the line current

is sufficient to pick up device 50, an undesired trip will occur.

Mitigation of this problem is to be aware of the possibility of unexpected de-assertion of inputs due to momentary loss of dc power during short circuits on other parts of the dc system. For this specific example, the current detector could be set higher than load current, or the sense of the line disconnect auxiliary switch input could be reversed so that loss of the input blocks the stub bus protection function.

VII. Conclusion

Power system transients have been classified into primary and secondary groups. Within each group there are well recognized (infamous) transients and not so well recognized (insidious) categories.

In many cases satisfactory mitigation of the impact of all types of transients is feasible. In some cases finding the optimum mitigation action may require simulation or playback of the transient phenomenon so that relay performance in the presence of the transients may be investigated. However if the transient phenomenon and impact on the protection is sufficiently well understood, previous research work will have identified the optimum mitigation method.

Several less well understood insidious transients have been described, and mitigation techniques presented. However, there is no end to the learning that experience can deliver. The authors hope that their experiences will be of interest and value to protection and power system analysis engineers.

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