Voltage Source Converter modeled in RTDS – experiences and comparison with field results

Tomas Larsson, Jean-Philippe Hasler, Paul Forsyth, Trevor Maguire

Abstract—For the first time it has been possible to model a three-level Voltage Source Converter (VSC) and test the physical firing pulse controls using a Real Time Digital Simulator (RTDS®). The new RTDS model is more flexible and comprehensive than both earlier digital versions and analogue TNA models. This allows more tests to be conducted in a shorter time and provides a more detailed power system representation for the tests. Using the new system to test the controls also simplifies the recording of results since all signals can now be gathered by the RTDS Simulator.

For the case of Electric Arc Furnace (EAF) compensation, the new real time digital simulation has made it convenient and easy to demonstrate the flicker improvement factor provided by the actual VSC controls under realistic system conditions.

The paper compares results from off-line and real time RTDS simulations, as well as from field measurements taken at a full scale ABB SVC Light® installation. The good correlation between simulation results and field measurements give confidence to the digital modeling.

Keywords: Power electronics, Power system simulation, Pulse Width Modulation, Real time simulator, Static VAR compensators.

I. NOMENCLATURE

EAF	Electric Arc Furnace
FACTS	Flexible AC Transmission System
PWM	Pulse Width Modulation
RTDS	Real Time Digital Simulator
SVC	Static Var Compensator
VSC	Voltage Source Converter

II. INTRODUCTION

SIMULATION of FACTS (Flexible AC Transmission Systems) devices is an essential tool in research, development and project related work. FACTS comprises a family of devices, constructed using state of the art computerized control systems in conjunction with high-power electronics. Typically FACTS solutions are justified where the application requires one or more of the following characteristics:

- Rapid response
- Frequent variations of output
- Smoothly adjustable output

Through simulation, solutions can be tested during steady state as well as during transient and fault conditions. The alternative of performing similar tests on a real plant is strongly limited due to technical and economical concerns.

Both off-line and real time simulation packages are available. Off-line simulations are most often performed using standard computers. For state of the art real time simulations, dedicated computer equipment with parallel processing capability is required.

Until recently the real time digital simulation of FACTS devices was limited to 2-level systems with a Pulse Width Modulation (PWM) frequency of less than 1 kHz. However, developments in simulation technology have made it possible to execute the demanding real time simulation of multi-level VSC converters with PWM switching frequencies in the order of 1.5 - 2 kHz.

III. RTDS DEVELOPMENT

A. Small timestep technique

Previously, VSC converters modeled in the RTDS Simulator were restricted to 2-level fixed topology configurations. It was recognized as desirable to allow user configured valve topologies and to be able to accommodate multilevel converters. A technique explored by Hui and Christopoulos, whereby the Dommel network conductance does not need to be decomposed or inverted during the simulation, was implemented [1, 2]. The difficulty with the technique is that it requires a simulation timestep in the order of 1-3 μs.

The technique represents the valve on-state impedance as a small inductance and the off-state as a large capacitance. The values of the inductor and capacitor are chosen such that they have the same conductance when represented using the Dommel algorithm, thereby allowing the difference in the on- and off-state behavior to be represented by changing only the respective current injection. The relatively small timestep is required to maintain a high ratio between the on- and off-state impedance of the valve.

Since the technique uses such a small timestep, no additional methods were applied to improve the valve firing instant. However, as presented below, great care was given to

T. Larsson is with ABB Power Systems, Västerås, Sweden (e-mail: tomas.x.larsson@se.abb.com).
J.-P. Hasler is with ABB Power Systems, Västerås, Sweden (e-mail: jean-philipe.hasler@se.abb.com).
P. Forsyth is with RTDS Technologies, Winnipeg, Canada (e-mail: paf@rtds.com).
T. Maguire is with RTDS Technologies, Winnipeg, Canada (e-mail: tlm@rtds.com)

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ensure low latency interaction with external firing pulse controls.

Simulating the VSC converters with the small timestep requires considerable hardware resources and limits the complexity of the components modeled in real time. Therefore, it was decided to adopt a dual timestep approach whereby the VSC is simulated with a small timestep (i.e. 1-3 μs), but the larger power system is represented with a timestep of approximately 50 μs. The two solutions are numerically interfaced in a manner similar to the techniques used to interface state variable models (e.g. dq0 synchronous machine model) to a time-domain simulation.

B. Hardware development

The implementation of the small timestep VSC simulation required the development of a new high speed processor card and low latency Input/Output (I/O) devices.

The Giga Processor Card (GPC) was developed to provide the computational power required for the small timestep simulation. The GPC card includes two IBM 750GX double-precision RISC processors operating at 1.0 GHz. Using the power of the two GPC processors, VSC circuits with up to 30 nodes and 36 switching elements can be simulated using the small timestep technique and interfaced to larger simulation networks.

Additionally the GPC card was equipped with Giga Transceiver (GT) optical ports for communication to external I/O cards. The GT ports operate at 2 GHz to transfer large amounts of data on and off the GPC card very quickly.

The VSC firing pulse controls require analogue signals from the simulation. An optically isolated 12 channel analogue output card with 16-bit D/A converters was developed for this purpose. The analogue output card, referred to as the GTAO, is able to update all 12 channels every small timestep.

Firing pulses must also be input to the simulation from the controls. The GTDI digital input card was developed to read the firing pulses from the controller every 320 ns and transfer the information to the GPC card using the GT port.

The total latency, from the point of the external controller issuing the firing pulse, to the point where the resulting effect of the pulse can be seen in the relevant analogue output, is 4-5 μs. The comparisons below show that this minimal delay does not adversely effect the testing of the VSC firing pulse controls.

C. Incorporation of measurement data

The VSC control tested was designed to compensate an EAF load. Therefore the EAF had to be accurately represented in the RTDS simulation to properly test the controls. Representing the behavior of the EAF is quite challenging since it is very erratic and thereby extremely hard to simulate and predict. An EAF model is available for the RTDS Simulator, but it remains difficult to choose the parameters such that the model behaves in the same way as the particular EAF to be compensated.

A relatively common practice for representing an EAF in a simulation is to inject currents recorded from the operation of a real EAF. The recordings include instantaneous value signals for the bus voltage and the EAF phase currents throughout an entire melt-down cycle lasting approximately 30 minutes. The data recording files typically constitute in the order of several gigabytes.

To accommodate the playback of the large EAF data recordings, a new device called the GTNET was utilized. In essence, the GTNET provides a direct link between the RTDS simulation and an Ethernet LAN. Using the Playback firmware, the GTNET can read EAF data recording files from a PC hard drive and make the signals available in the real time simulation.

IV. THE SIMULATED SYSTEM

The tests and comparisons were made for a recent EAF compensation project that included an SVC Light from ABB [3]. The EAF is a source of several kinds of disturbances, which, unless remedied, results in strong deterioration of power quality. The main challenge is the large stochastic variations in reactive power consumption that give rise to large and rapid grid voltage fluctuations. Another power quality parameter affected by the EAF is unbalance.

The phenomenon flicker (i.e. annoying fluctuations in lighting levels) is inherently connected to variations in reactive power. To achieve a high level of flicker mitigation, it is necessary to use a fast reacting FACTS device such as ABB's VSC based SVC Light [4, 5, 6, 7]. This technology is also very effective in the reduction of unbalances.

The EAF installation used for the comparison was fed from the 220 kV grid by a 160 MVA transformer which stepped the voltage down for the industrial bus at 35 kV. The EAF, rated 140 MVA, was compensated by a 164 Mvar SVC Light realized by a three-level VSC of +/-82 Mvar and three filters with a total of 82 Mvar. The details are shown in Fig. 1.

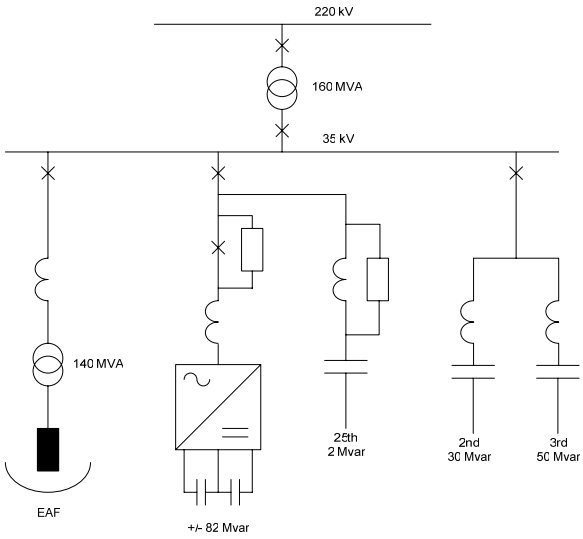

Fig. 1. Single line diagram of the studied installation

The IGBT based VSC was directly connected to the 35 kV industrial bus via a compact, three-phase set of air-core reactors. A charging circuit was installed between the 35 kV bus and the phase reactors. The charging circuit is an installation-dependent circuit and is not always required.

To achieve the required flicker mitigation level, the VSC had to operate at a sufficiently high switching frequency. In this case the switching frequency was 1650 Hz.

Fig. 2 shows a site photo of the SVC Light installation with the steel plant in the background.

Fig. 2. Site photo

V. Simulation Results

This section focuses mainly on flicker mitigation performance, but the unbalance reduction capability is also illustrated.

A. Off-line simulation

For flicker mitigation projects, it is of great importance to evaluate the performance of a compensator installation at the tender stage. The performance normally includes flicker mitigation, voltage quality, harmonic distortion and negative-sequence reduction.

To evaluate the performance, field measurements from a similar EAF are selected from a database. The field measurements are used in simulations performed by an electromagnetic transient simulation program such as PSCAD®/EMTDC®. The simulation model includes the source network, step-down transformer, harmonic filters and a complete representation of the compensator. The EAF itself is represented as a current source controlled by a data file of the field measurements.

The available EAF data recordings normally cover several days of operation, but normally only one typical melt-down cycle is selected for the simulations. One melt-down cycle takes approximately 20 minutes. Using EMTDC, and a conventional personal computer, such a simulation takes about one day to run.

Fig. 3 shows the results from the EMTDC simulation. The EAF real power is displayed in the first subplot and the EAF and step-down transformer reactive power are displayed in the second subplot. Fig. 3 shows that nearly all of the EAF reactive power is supplied by the compensator. The third subplot corresponds to "output 5" of the IEC flicker meter [8]. The Pst value, corresponding to the statistical value of the flicker level over a 10-minute window, is shown as a text label in the plot. The Pst value is computed outside of EMTDC using MatLab®. The last subplots show the EAF bus voltage and the negative-sequence currents from the EAF and the network transformer. The plots illustrate the low level of voltage fluctuation and the reduction of the current unbalance between the EAF and the network transformer.

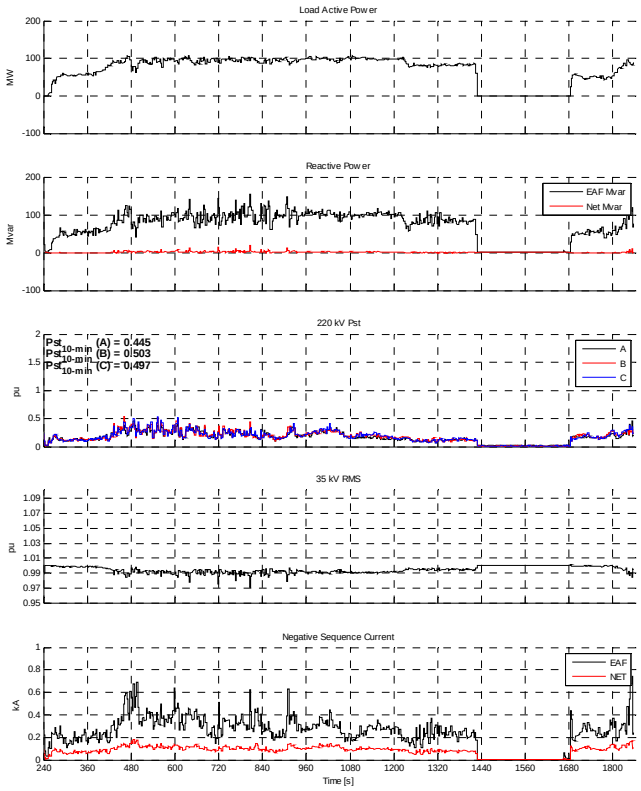

Fig. 3. EMTDC simulation at tender stage
a) EAF active power
b) EAF and step-down transformer reactive power
c) Flicker
d) Bus voltage
e) EAF and step-down transformer negative sequence current

B. On-line simulation

At the project stage, the actual control system (including all I/O interfaces) is tested using the RTDS Simulator. The RTDS model is identical to the model implemented in EMTDC, except for the control system which replaces the model with the physical controller. The simulator and the physical controller exchange signals, such as voltages, current and valve firing pulses through electrical connections. The data file containing the bus voltage and the EAF current are read by the GTNET's Playback firmware and made available in the RTDS simulation.

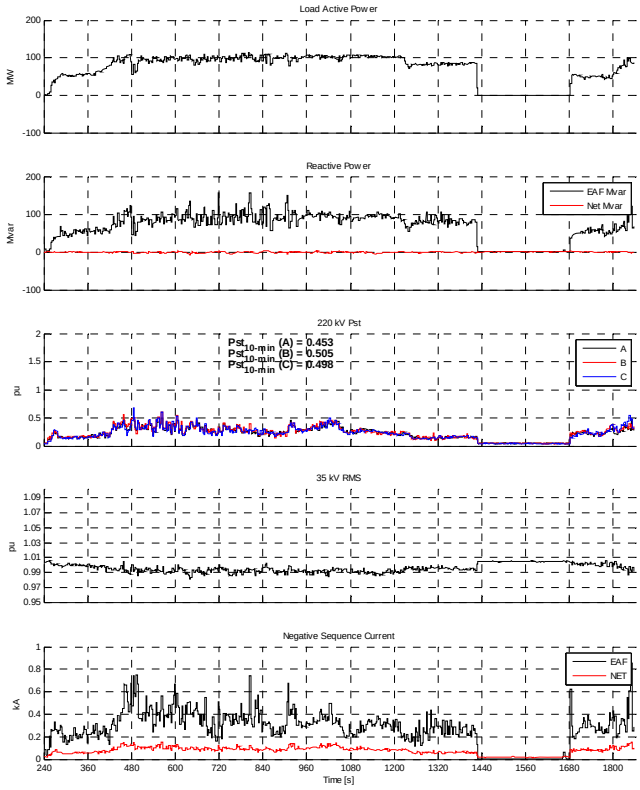

Fig. 4. RTDS simulation at project stage
a) EAF active power
b) EAF and step-down transformer reactive power
c) Flicker
d) Bus voltage
e) EAF and step-down transformer negative sequence current

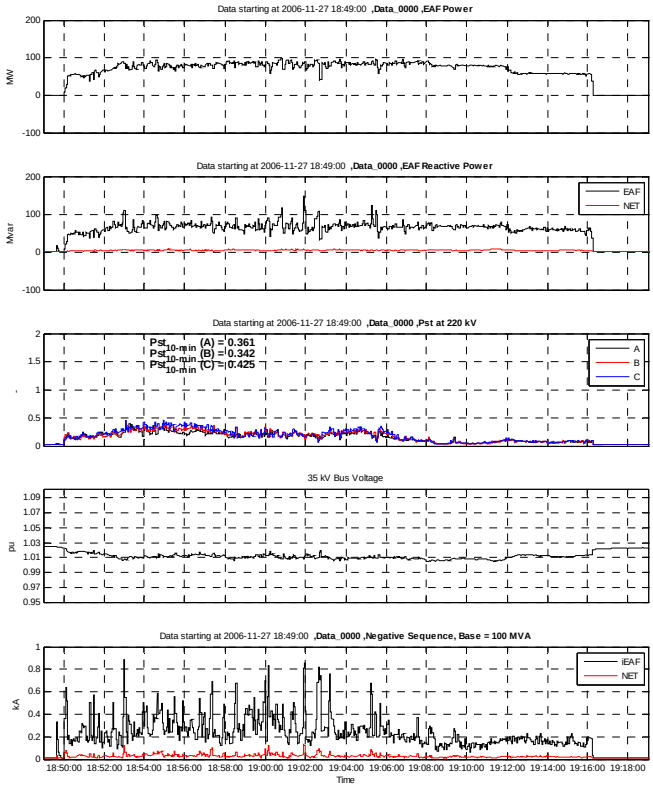

Fig. 5. Site measurement
a) EAF active power
b) EAF and step-down transformer reactive power
c) Flicker
d) Bus voltage
e) EAF and step-down transformer negative sequence current

Fig. 4 shows the results obtained with the RTDS simulation. It should be noted that the results were obtained in real time with RTDS (over approximately 30 min.) compared to EMTDC which requires about one day for the same simulation.

The specification of the control system is based on the EMTDC model and comparison between the EMTDC and RTDS simulation results should confirm the correct implementation of the control algorithm in the physical controls. Comparing Fig. 4 to Fig. 3 confirms that the results are very similar and indeed verifies that the control system performs according to the specification. At the same time, the results give confidence to the control system model in EMTDC.

RTDS testing was not limited to the flicker compensation performance. A large number of other case scenarios were tested using RTDS Simulator. A typical study case for an SVC Light installation is a ground fault in the DC circuit of the converter. To perform a staged fault onsite would be very difficult due to the limited time available for commissioning and due to safety concerns. When simulating such a fault, it is very important that the power system voltages and currents are reproduced as they would be in reality. This was very hard to achieve using an analogue Transient Network Analyzer (TNA) where the saturation phenomenon is difficult to reproduce. As an alternative to the TNA, EMTDC simulations were used. However, a tremendous effort was required to model all relevant parts of the control interface, such as interfacing transformers and protecting devices. Using the RTDS Simulator, not only can the control and protection algorithm be tested, but also all the control interface transducers which may be sensible to DC components and harmonics.

Extensive testing of the control and protection system, including the interposing transducers and relays, considerably reduces the commissioning period of such an installation. This is an important factor since the time allowed for commissioning of an industrial compensator is often limited to avoid interference with steel production. The first SVC Light installations tested with the RTDS Simulator have had a reduction of the time needed for commissioning. Furthermore, the possibilities for troubleshooting have been improved.

C. Site measurements

Fig. 5, shows the same signals as Fig. 3 and 4, but from onsite measurements. The data was recorded with a 16-channel synchronously sampling device and stored on a hard disk for off-line post processing of the power quality parameters according to the IEC standard.

Fig. 5. shows the results from one melt-down cycle. Comparing the onsite results with the simulations performed earlier shows a slightly lower EAF power, but still demonstrates a very well compensated installation. The measured flicker results were even slightly better than the initial estimates. This may result from the increased stability of the bus voltage provided by the compensator.

The reduction of EAF unbalance currents was better than expected even though the load unbalance was larger than simulated in the model. The large reduction of unbalance is a feature of SVC Light which is not possible to achieve using classical thyristor technology.

VI. Conclusions

The paper describes new developments in the RTDS Simulator with particular focus on the simulation of multi-level VSCs using PWM control.

Results from three different environments have been shown; off-line simulation, real time simulation, and onsite measurements of a 164 Mvar SVC Light installation. Comparing the results shows very good conformity between the two simulation environments and the site measurements.

The work conducted clearly shows that the RTDS Simulator can be relied upon to accurately test VSC firing pulse controls using PWM frequencies in the range of 1500 Hz. Furthermore, the value of the real time simulator for research and development, as well as for factory verification testing, of VSC controls was demonstrated.

VII. References

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VIII. Biographies

Tomas Larsson received his M.Sc. in Electrical Engineering in 1991 and his Ph.D. in High Power Electronics in 1998, both from the Royal Institute of Technology in Stockholm, Sweden.
Mr. Larsson joined ABB in 1998 where he presently is involved in projects concerning Voltage Source Converters, reactive power compensation and flicker mitigation.

Jean-Philippe Hasler received his M.Sc. degree in Electrical Engineering from the Ecole Polytechnique Federale de Lausanne, Switzerland in 1986.

Mr. Hasler joined ABB in 1986 where he was developing control systems and protection algorithms for multi-terminal HVDC. Since 1993 he is conducting power system and control studies for different FACTS applications.

Paul Forsyth received his B.Sc. degree in Electrical Engineering from the University of Manitoba, Canada in 1988. After graduating he worked for several years in the area of reactive power compensation and HVDC at ABB Power Systems in Switzerland. He also worked for Haefely-Trench in both Germany and Switzerland before returning to Canada in 1995. Since that time he has been employed by RTDS Technologies where he currently holds the title of Marketing Manager / Simulator Specialist.

Trevor Maguire graduated from the University of Manitoba with B.Sc.EE, M.Sc.EE and Ph.D. degrees in 1975, 1986, and 1992 respectively.
Relevant employment experience includes time with Manitoba Hydro (1975-76), Manitoba HVDC Research Centre (1986-1994), and RTDS Technologies, Inc. (1994-present). He is a founding principal of RTDS Technologies, Inc. with a special interest in real time simulation model development and also real time simulation digital hardware development. He participated in creating the world’s first commercial real time digital power system simulator.