

Efficient and Accurate Multirate Simulation of HVDC Converters in a Partitioned Network Environment

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Abstract—Multirate simulation of electric networks exhibiting a wide variety of time constants decreases the simulation runtimes by exploiting the property of circuit latency. The fundamental idea is to use different integration steps for distinct elements and/or parts of the network according to requirements of accuracy for each element. HVDC converters are ideally suited for latency exploitation since the differences in step size requirements are well defined. This paper presents the recent developments for an efficient and accurate circuit latency exploitation as well as the results obtained when a twelve-pulse HVDC converter is simulated using this technique. Latency is exploited using direct integration methods instead of the traditional iterative methods, making the approach suitable for real-time simulation. Comparisons are made with the traditional single step solution in order to emphasize the accuracy and efficiency of the proposed method.

Keywords: Circuit latency exploitation, diakoptics, integration rules, multirate simulation, EMTP, HVDC.

I. INTRODUCTION

THE “Electromagnetic Transients Program” (EMTP) [1,2] in its several versions has been used for many years for the simulation of electromagnetic transients in “High Voltage Direct Current” (HVDC) transmission systems. The modeling detail allowed by the EMTP combined with its time domain solution method guarantees very accurate solutions when simulating high frequency transients, DC link faults, and commutation failures, for example.

One of the limitations of conventional EMTP-type simulators, however, is their incapability of performing real-time simulations which are particularly important in HVDC transmission system studies. The main purpose in this case is the simulation in closed-loop of the converter control using as

input data the results obtained through digital simulation.

Several research groups have been actively pursuing the development of real-time simulators [3-5] and currently there are many options available in the market. However, the cost of many of these simulators is still quite prohibitive, especially for academic institutions. One of the reasons for the high cost of the simulators is the necessity of a very powerful hardware platform specifically dedicated to the simulator. The hardware is normally organized in individual interconnected racks adjusted to a certain network configuration. This method introduces another important limitation of such simulators since performing modifications in the network configuration may be a time consuming task.

In previous works, we have presented a very efficient simulation method based on the exploitation of circuit latency by which different integration steps may be simultaneously used for the full network solution [6,7]. In conventional EMTP solutions, the same integration step is used for all parts of the network and its size is determined by the solution needs of the “fastest” subsystem (smallest Δt needed). This quite often results in a waste of computational resources since the step size may be unnecessarily small for other subsystems that vary at a pace significantly slower than the faster subsystems.

HVDC converters are ideally suited for latency exploitation since small integration steps should be used for the converter bridges while the rest of the network may be simulated with a much larger time step without loss of accuracy. This multirate solution technique may eventually allow the real-time simulation of HVDC converters in low cost workstations.

The paper is organized as follows. Section II gives an overview of the multirate solution technique while in section III the modeling of the HVDC converter that will be analyzed in the paper is presented. In section IV, simulation results are presented and finally conclusions are stated in section V.

II. OVERVIEW OF THE MULTIRATE SOLUTION TECHNIQUE

A. The Multi-Area Thévenin Equivalent (MATE) Partitioning Technique

As a framework for the network partitioning performed in order to separate the original network into two or more subnetworks that can be simulated with distinct integration

This work was supported by the Fundação de Amparo à Pesquisa do Estado de São Paulo (FAPESP), Brazil.

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steps, the MATE technique [8] is employed. MATE is based on the old diakoptics technique [9] by which the solution of a large system may be obtained by first tearing the system across some branches, forming smaller subsystems which are then solved initially as if they were completely independent. The torn branch currents are calculated and finally the full system solution is obtained by injecting back the branch currents into the separate subnetworks. Fig. 1. shows an example network from which the basics of MATE's solution can be indicated.

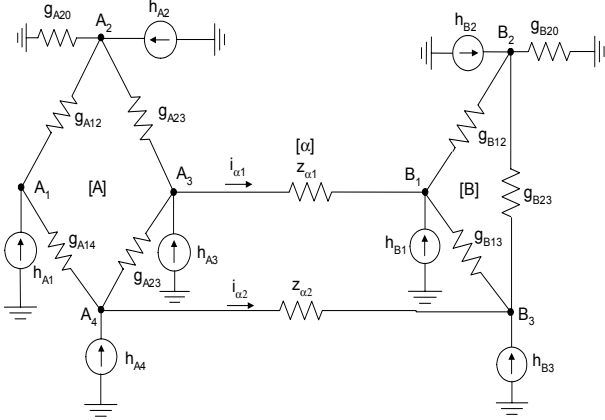


Fig. 1. Sample network for MATE explanation.

The following notation is introduced:

$[A]$ = admittance matrix of subnetwork A;

$[B]$ = admittance matrix of subnetwork B;

$[\alpha]$ = links connecting subnetworks A and B;

$i_{\alpha 1}$ = current in link branch α_1 ;

$i_{\alpha 2}$ = current in link branch α_2 ;

$z_{\alpha 1}$ = impedance of link branch α_1 ;

$z_{\alpha 2}$ = impedance of link branch α_2 ;

h_A and h_B are the current sources injected from ground into the nodes of subnetworks A and B respectively.

For MATE solution the following procedure should be adopted:

1. Obtain the steady-state solution of the complete network (at $t = 0$);
2. Build the admittance matrices for subnetworks A and B as if they were completely independent;
3. Advance the solution time by $t = t + \Delta t$;
4. Update the history sources terms for subnetworks A and B;
5. Solve for the internal node voltages of subnetworks A and B, still considering both completely decoupled;
6. Solve for the link currents $i_{\alpha 1}$ and $i_{\alpha 2}$ using the node voltage values calculated in step 5;
7. Update the internal node voltages of subnetworks A and B by injecting the link currents $i_{\alpha 1}$ and $i_{\alpha 2}$ into the corresponding nodes;
8. Go back to step 3 until $t = t_{max}$.

The node voltages calculated in step 5 are actually the Thévenin equivalent sources for subsystems A and B (hence the acronym MATE) and the interaction between subnetworks

occurs when injecting the link currents into the corresponding nodes. The internal node voltages are then precisely calculated in step 7.

B. Basics of Latency Exploitation under MATE's Framework

MATE's solution scheme allows the network partitioning to be performed along boundaries of maximum solution efficiency. One important example is the simultaneous solution of systems discretized with different step size Δt for multirate simulation as discussed in section I.

In our latency approach the large time step should always be an integer multiple of the small one,

$$\Delta T = n \Delta t \quad (1)$$

where n is a positive integer, larger than unity, and ΔT and Δt are the large and small time steps, respectively.

Fig. 2 shows the timeline of the simulation at a general time interval.

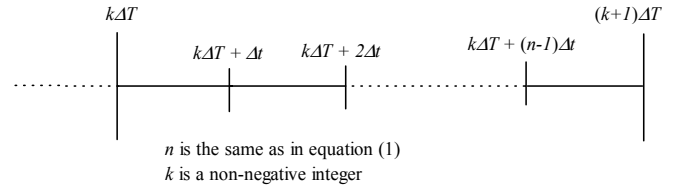


Fig. 2. Timeline of the simulation at a general time interval when latency is exploited.

There have been some attempts to exploit circuit latency in the time-domain simulation of "Very Large Scale Integration" (VLSI) circuits and power systems using the "waveform relaxation" (WR) method [10,11]. WR, however, is an iterative procedure where each subsystem uses the previous iterate waveforms as "guesses" for the current state of the other subsystems. This approach is simply not suited for real-time simulation since it does not provide for a simultaneous solution of the links connecting the various subsystems. In this work, latency is achieved using robust implicit integration methods like trapezoidal and backward Euler.

Although theoretically simple, the simulation of a network using different integration steps is not trivial. The interface between the "fast" and "slow" subsystems has to be adjusted in order to guarantee an accurate and efficient simulation. Incorrect approaches in the coupling of the subsystems may lead to strong numerical oscillations and divergence of long-term simulation. In [6,7] the details of the coupling between the subsystems have been presented. The two basic concerns are

- How to consider the contribution of the slow-varying subsystem (the latent one) when solving only for the fast-varying subsystem, and
- How to evaluate the contribution of the fast-varying subsystem through a complete ΔT interval for the slow-varying subsystem solution.

1) Thévenin Equivalent Interpolation of the Slow Subnetwork for the Solution of the Fast Subnetwork

Fig. 3 shows the Thévenin equivalent representation of the network divided into slow and fast subsystems according to the MATE partitioning technique.

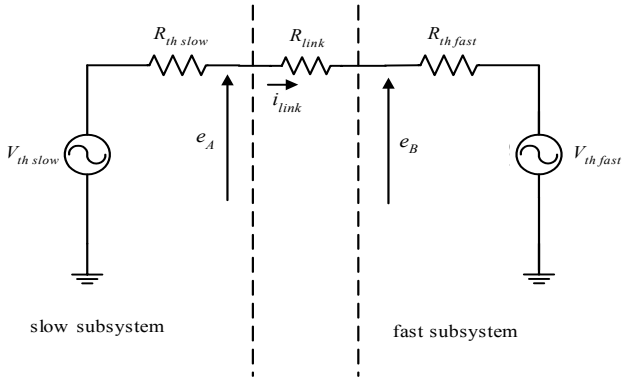


Fig. 3. Thévenin equivalent representation of slow and fast subnetworks at linking nodes.

In this network representation R_{thslow} and R_{thfast} are constants and are respectively the Thévenin equivalent resistances of the slow and fast subnetworks. On the other hand V_{thslow} and V_{thfast} change at each time step and are respectively the Thévenin equivalent voltage sources of the slow and fast subnetworks. These equivalent voltage sources represent the combined effects of the independent voltage and current sources and the history sources in each subnetwork. Independent voltage and current sources are a known function of time and the history sources are update from the last calculated solution. The evaluation of V_{thfast} is therefore quite straight forward since the last calculated solution was at the instant $t - \Delta t$. In the case of V_{thslow} the situation is a little bit different. It is not possible to determine its exact values at each time step Δt , since the variables of the slow subnetwork are only calculated at every large step ΔT . Nevertheless, it is possible to perform a linear interpolation on V_{thslow} . Suppose that the whole network has been solved at time “ t ”. It is possible to obtain the Thévenin equivalent voltage source V_{thslow} at $t + \Delta T$ since it can be expressed as a function of the independent voltage and current sources and history sources:

$$V_{thslow(t+\Delta T)} = f(\mathbf{v}_s(t+\Delta T), \mathbf{i}_s(t+\Delta T), \mathbf{e}_{hs}(t+\Delta T)) \quad (2)$$

where $\mathbf{v}_s(\cdot)$ is the vector of all independent voltage sources, $\mathbf{i}_s(\cdot)$ is the vector of all independent current sources and $\mathbf{e}_{hs}(\cdot)$ is the vector of all history sources within the subnetwork. The history sources determined at $t + \Delta T$ only depend on the node voltages and branch currents at instant “ t ” as in

$$\mathbf{e}_{hs}(t + \Delta T) = \mathbf{g}(\mathbf{v}(t), \mathbf{i}(t)) \quad (3)$$

where $\mathbf{v}(\cdot)$ is the vector of known node voltages and $\mathbf{i}(\cdot)$ is the vector of known branch currents. By evaluating (3) and substituting it in (2), V_{thslow} at the instant $t + \Delta T$ can be calculated. Finally, for each small time step Δt within the large step ΔT , V_{thslow} is calculated by linearly interpolating between $V_{thslow}(t)$ and $V_{thslow}(t + \Delta T)$. The link current i_{link} is then calculated as

$$i_{link} = \frac{e_A - e_B}{R_{link}} \quad (4)$$

where e_A and e_B are as shown in Fig. 3. In Fig. 4, the network representation of Fig. 3 is repeated but now with the indication of how each network component is evaluated when only the fast subnetwork is solved. Applying this interpolation to the Thévenin equivalent voltage source of the slow subnetwork prevents it from being considered as completely dormant, since in fact it is varying slowly, but continuously.

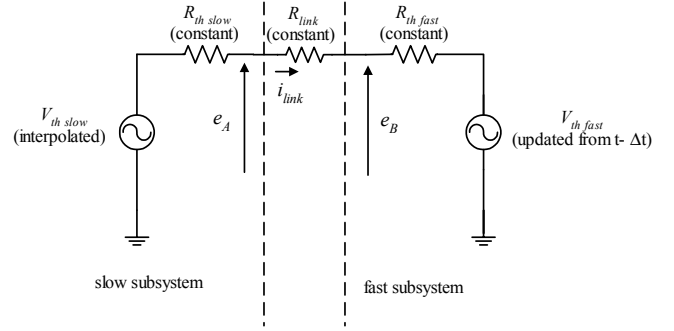


Fig. 4. Indication of how each network component is calculated when only the fast subnetwork is solved in detail.

2) Double Link Current Injection at Resynchronized Solution Points

Whenever it is time to solve for the entire network (at every instant multiple of the large time step ΔT) the history sources are updated from the solution at $t - \Delta t$ for the fast-varying subnetwork, and from the solution at $t - \Delta T$ for the slow-varying subnetwork. However, the fast subsystem has been calculated “ n ” times, according to (1) trough a complete ΔT cycle. The last calculated solution at $t - \Delta t$ is therefore not representative of the fast subsystem’s variation from the viewpoint of the slow subsystem. Calculating an average of the solution of the fast subsystem variables through the complete ΔT cycle would be more accurate for the solution of the slow subsystem. This procedure however, would require many operations defeating the very purpose of latency exploitation. A compromise solution may be reached by averaging only the Thévenin equivalent voltage source of the fast subnetwork V_{thfast} (which is a fast variable anyway), using it to update the node voltages of the slow subnetwork.

The way to implement this solution is to perform a double system update at instants of resynchronization. The history sources of the fast components are updated from the solution obtained at $t - \Delta t$, i.e., from the last calculated solution for this part of the network. Different link currents are then evaluated according to the part of the network that is going to be solved. For the fast subnetwork solution the link current is simply calculated according to (4). However, for the slow subnetwork, first the average of V_{thfast} is obtained through a complete ΔT cycle, so that the variation of the fast-varying elements during this cycle is taken into account. This approach prevents the quasi-randomness of taking into account only the single value of the last calculated solution of the fast subnetwork. This average of V_{thfast} ($V_{thfast-ave}$) is calculated as follows:

$$V_{thfast-ave} = \frac{\sum_{k=1}^n V_{thfast}(t - \Delta T + k\Delta T)}{n} \quad (5)$$

The link current that is going to be injected into the slow subsystem is now calculated with V_{thfast} substituted by $V_{thfast-ave}$. Fig. 5 illustrates the situation.

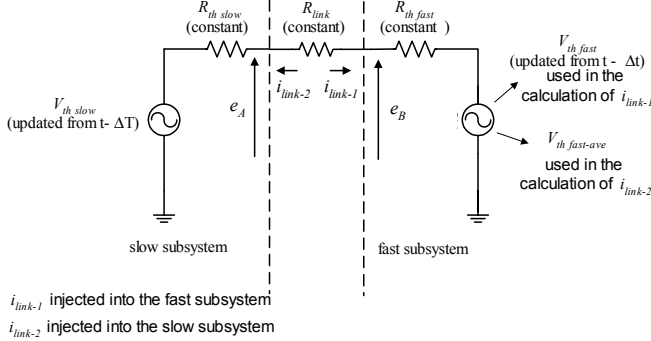


Fig. 5. Network representation for complete network solution.

III. MODELING OF THE HVDC CONVERTER

A. Modeling of Diode-Type Elements

EMTP models diode-type elements such as diodes and thyristors as ideal switches that either conduct or block depending on its polarization. Although neglecting the internal characteristics of the switching devices, this approach is usually sufficient for simulations at the system level as usually performed in power systems transients analysis. The approach followed by the EMTP is to either collapse or create nodes depending on whether the device is on its conducting or blocking states. This procedure requires the retriangularization of the conductance matrix whenever a switch changes its state.

On the other hand it is possible to keep the dimension of the conductance matrix constant if the switch is modeled as a resistance that is either very small when closed or very large when opened [12]. By maintaining the size of the conductance matrix constant, it is possible to pre-calculate and pre-store all the possible combinations of the switches for each HVDC bridge. This is of major importance for an efficient simulation of the full HVDC converter by way of the MATE technique, as shall be discussed later.

In this work the switches are considered as simple diodes, therefore no control circuit was implemented in order to generate a firing signal. For the purpose of this paper, it is enough to consider the switches in this way. However, the authors expect to present some results with thyristors as switching devices in the near future.

B. Modeling of Transformers

The YY and YΔ transformers are modeled as three ideal single phase units, in series with their short-circuit reactance to take into account the non-ideal commutation of the diodes. Saturation has not been taken into account in this work.

C. Other Modeling Considerations

The smoothing reactor used to filter out the harmonic

content in the DC line current has been included in the simulations.

The AC and DC filters are not represented in this study but their inclusion is quite straightforward. In order not to increase the number of nodes excessively the filters may be modeled as equivalents of series/parallel RLC combinations.

The generators are represented as ideal sources behind an impedance and the rectifier feeds a resistance representing the DC line. A constant voltage source is used for the simplified representation of the inverter.

D. MATE Partitioning of the HVDC System for Latency Exploitation

With the MATE formulation of the diakoptics technique, the HVDC converter system can be divided into several subsystems interconnected by some link branches, as explained in section II. Fig. 6 shows the HVDC converter under analysis with the indication of the branch tearings performed.

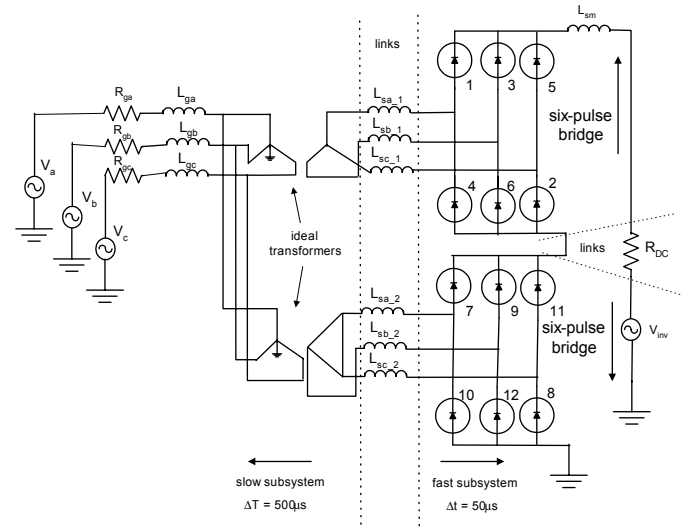


Fig. 6. HVDC rectifier station.

The diodes are numbered in their traditional firing sequence for each of the six-pulse bridges. To correctly represent the dynamics of the switching valves, a time step of 50μs is usually adopted to correspond to approximately one electrical degree. As indicated in Fig. 6, the AC part of the network is the slow subsystem and is going to be simulated with a time step of 500μs, while the bridge itself is simulated with the time step of 50μs. Another partitioning is performed in order to separate the two six-pulse bridges as also indicated in Fig. 6. The advantage of this other segmentation level is that the inverse conductance matrices corresponding to all possible valve combinations may be pre-calculated and stored in computer memory [12]. Each of the six-pulse bridges is constant changing states. Assuming only single commutation, there are 12 possible valve combinations (only two and three valve conduction modes) for each bridge. There are potentially many other possible states however, since four valve conduction modes (double-commutation) in each bridge may also occur during DC line faults and dips in AC voltage.

By pre-calculating all the possible conductance matrices there is no need to retriangularize the bridge matrices whenever a switch changes state. The pre-inverted matrix is simply picked up from computer memory based on the results of the previous solution step. This saves computational effort during the transient solution.

IV. TEST CASE

Circuit data for the converter represented in Fig. 6 are indicated in Table I. The AC source is symmetrical and the frequency is 60Hz. The backward Euler integration rule was adopted for the simulations since it does not introduce numerical oscillations at discontinuities, being of critical importance in the simulation of power electronics devices. Another option would be to implement the CDA procedure [13]. For simplicity reasons, however, this option was not adopted in the code implementation of the latency enabled simulator. The diodes have been represented as a very low resistance (0.1mΩ) when conducting and as a very high resistance (1GΩ) when blocking.

TABLE I
NETWORK PARAMETERS FOR THE NETWORK SHOWN IN FIG. 6

Component	Value
$V_a = V_b = V_c = V_s$	162 kV
V_{inv}	484 kV
$R_{ga} = R_{gb} = R_{gc} = R_g$	2 Ω
$L_{ga} = L_{gb} = L_{gc} = L_g$	100 mH
$L_{sa1} = L_{sb1} = L_{sc1} = L_{sa2} = L_{sb2} = L_{sc2} = L_s$	100 mH
L_{sm}	0.7 H
R_{dc}	5 Ω

Fig. 7 presents the three-phase and the rectified voltages obtained.

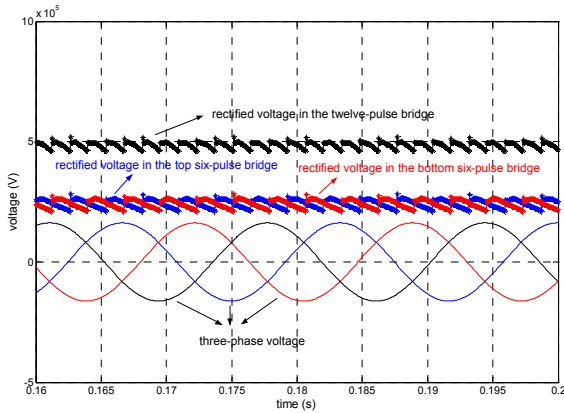


Fig. 7. Three-phase and rectified voltages ($\Delta T = 500\mu s$ and $\Delta t = 50\mu s$).

For comparison, Fig. 8 presents the same variables obtained when a single step of 50μs is used.

It can be seen that the results agree very well, except for some of the spikes that appear in the rectified voltages which are due to the impossibility of exactly detecting the instants when commutation ceases. Over the past few years there have been many contributions in order to solve this problem, usually based on linear interpolation of the current through the diodes so as to detect the zero crossings as precisely as

possible [14,15]. Its analysis, however, is beyond the scope of this paper. Fig. 9 presents the current commutation between diodes 1, 3, and 5 for the double time step method, whereas Fig. 10 presents the commutation for the single time step case.

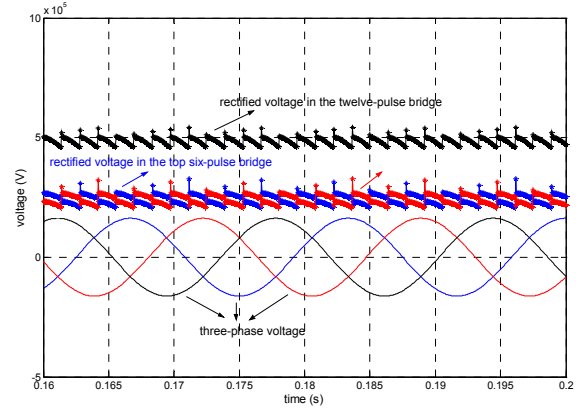


Fig. 8. Three-phase and rectified voltages (single time step: $\Delta t = 50\mu s$).

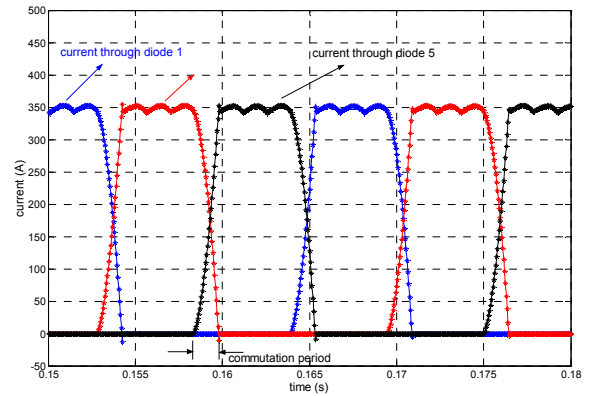


Fig. 9. Current in diodes 1, 3, and 5 ($\Delta T = 500\mu s$ and $\Delta t = 50\mu s$).

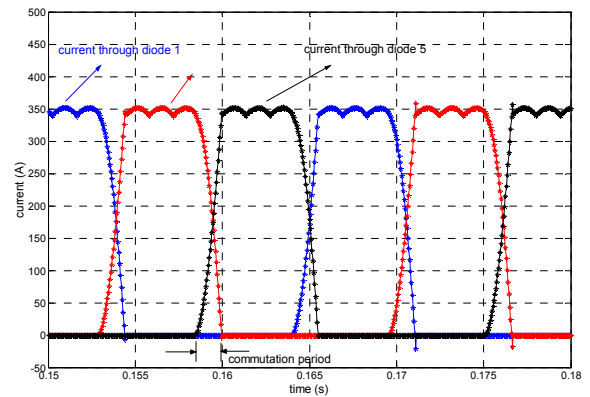


Fig. 10. Current in diodes 1, 3, and 5 (single time step: $\Delta t = 50\mu s$).

Once again the results show a very good agreement. Latency exploitation has therefore been validated in terms of accuracy.

Latency should now be addressed in terms of efficiency when compared to the conventional EMT-type single step simulation. Table II shows the CPU time in order to execute the simulation up to 0.2s using a Pentium III, 1.1GHz PC. The codes have been written in MATLAB version 6 both for the double step and single step cases for fairness of comparison.

TABLE II
CPU TIME FOR SINGLE AND DOUBLE TIME STEPS METHODS

Method	CPU time (s)
Single time step	63.3
Double time step	34.3

The double time step method is approximately 85% faster than the single time step case. A much more significant reduction can be expected for larger networks, like, for example, a bipolar HVDC transmission link where both rectifier and inverter were represented, as well as the AC and DC filters. The implementation of such systems is currently under way and the authors expect to have some results in the near future.

It should be mentioned that the simulation of the complete network with a time step of 500 μ s would only provide accuracy to about 10 electrical degrees for the switching devices, a value completely unacceptable for the simulation of converter stations.

V. CONCLUSIONS

This paper proposed latency exploitation within the context of partitioned networks for the simulation of HVDC converters. The network partitioning follows the approach provided by the new formulation of the diakoptics technique known as MATE, which allows an ideal framework for circuit latency exploitation.

In the methodology presented, the contribution of the slow part of the network is taken into account at instants when solving only for the fast part by an interpolation of the Thévenin equivalent voltage source of the slow subnetwork, a procedure that is numerically stable. Also, the variation of the fast subsystem through a complete ΔT cycle is accounted for when solving for the slow subnetwork through the averaging of the Thévenin equivalent voltage source of the fast subnetwork.

Circuit latency has been exploited using robust direct integration methods (in this case backward Euler) instead of the iterative methods, making the approach well suited for future real-time implementation.

The case of a twelve-pulse rectifier station has been presented. Accuracy was maintained at the same time that there was a gain of approximately 85% in the simulation speed when employing the double time step solution method compared to the single time step EMTP-type solution.

For future work, the authors are considering latency exploitation in complete HVDC bipolar systems, as well as in FACTS controllers where the time step requirements are even more stringent due to the very high switching frequency of available “pulse width modulated” (PWM) inverters.

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VII. BIOGRAPHIES

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