Accurate Solution of HVDC Converters in Real Time Transients Simulation

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Abstract—**A very efficient model has been developed to represent High-Voltage Direct Current (HVDC) Converters in real-time transient simulators. Real time performance of 46 μs per solution step has been achieved for a 12-pulse monopolar converter and 81 μs for the bipolar converter using an inexpensive off-the-shelf Pentium Pro 200 MHz desktop computer. The converter model is solved simultaneously with the power network, making it valid for continuously running real-time power system simulators. The Critical Damping Adjustment (CDA) technique is used to provide numerically clean and accurate waveforms.**

Keywords: Real-time power system simulators, HVDC converters, high-voltage, direct current, EMTP solution techniques, power electronics device modelling.

I. INTRODUCTION

The power systems research group at the University of British Columbia (UBC), Microtran Power system Analysis Corporation, and Mitsubishi Electric Corporation have been actively involved in the development of fast and accurate algorithmic solutions for real-time transients simulation [1], [2], [3]. This paper describes cooperative work in developing a high-performance model for 12- and 24-valve HVDC converters suitable for real-time power system simulators.

The test model presented here includes a simplified AC source network representation, converter transformers, converter bridges, and smoothing reactors. Fig. 1 shows a typical converter substation. The full model will include a full power network representation as well as other details like harmonic filters.

The task of developing an efficient 12-pulse converter substation model that can perform under the constraints of real time (e.g., around 50 μs per solution step) and can be solved simultaneously with the power network is a particularly challenging task. Traditional EMTP modelling techniques are not sufficient in this case.

The EMTP models diode-type elements, such as, diodes, thyristors, GTO's, etc. as switches that ideally conduct or block depending on the polarization signals. This approach ignores the internal details at the device level, but it is widely accepted as sufficient for power electronic devices at the circuit level [4].

The traditional EMTP technique of collapsing or creating nodes as the device conducts or blocks involves retriangularizing the system's [G] matrix whenever there is a change in the conducting state of one of the valves [5]. In a 12- or 24- valve converter, however, this process is simply too slow for real time performance.

Another major difficulty in modelling diode-type devices in transient simulations is the numerical oscillations of the trapezoidal rule of integration whenever current is interrupted in an inductive circuit. These undamped oscillations occur even if interruption takes place at a natural zero crossing of the current, and can render the results of a power electronics simulation totally useless both in terms of valve misfirings due to noisy signals and in terms of output signals.

The HVDC converter model developed in this project has succeeded in overcoming the above-mentioned problems and has resulted in a fast and accurate model suitable for real time simulation. The algorithm is written in portable C++ code using object-oriented programming techniques. On a first stage, the model has been tested using a desktop Pentium Pro 200 MHz computer. The object-oriented structure of the code, however, permits its easy porting to parallel-computer architectures. Work is currently in progress to implement the algorithm in high-performance parallel-processing machines.

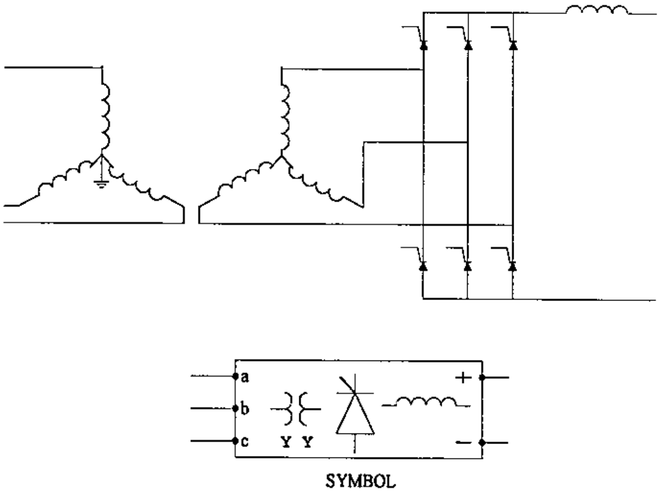


Fig. 1. HVDC Converter Substation

II. HVDC CONVERTER SUBSTATION MODEL

The model of an HVDC converter substation includes the power transformer, the rectifier or inverter, and the smoothing reactor. Fig. 1 shows the substation when using a Y-Y transformer.

The transformer model used here consists of three single-phase units, each one modeled as an ideal transformer in series with its short circuit impedance [5]. In the discrete time domain it is possible to write the transformer admittance matrix directly from the nominal data. Because an ideal transformer is perfectly coupled, this matrix has no inverse. However, when forming the converter substation matrix, the valve's conductances are added providing the necessary non singularity to the matrix. The three-phase bank is formed using three units and specifying if the connection is Y-Y or Y-Δ.

In order to maintain the dimension of the sub-matrices constant, the thyristor valves are modeled as varying resistors. A very low resistance is used for the conducting state and a very high resistance for the off state. The holding current Ih, and the minimum turn on voltage Von are user defined.

The smoothing reactor, commonly used in HVDC systems to filter the harmonics content in the dc line current, is modeled as an inductor and its equivalent is added to the converter substation matrix together with the corresponding valves and transformer conductances.

III. SOLUTION ALGORITHM

As indicated, a major obstacle in developing a real time HVDC converter model is the efficiency of the algorithm.

The experience in developing UBC's Real-time Network Simulator (RTNS) [1] indicated that pre-calculation and pre-storage of the inverse conductance matrix $[G]^{-1}$ for all possible conducting states of the switches could result in very efficient execution speeds. In the present problem, however, for 24 valves there are $2^{24} = 16{,}772{,}216$ possible conductance matrices. Considering both rectifier and inverter, the number of pre-stored matrices would be in the order of 33 million. This number was considered excessive for a general converter model solution.

To overcome the problem of modelling all valves as a single matrix, with the excessive number of possible combinations indicated above, it was decided to follow an object-oriented approach and reduce the problem to more manageable units. In the adopted approach, each bridge (6 valves), together with its associated power transformer, is considered as a single object and all possible states of this object are pre-calculated. This means a maximum of 64 states per bridge (the actual number is slightly smaller because not all possible conducting-state combinations are physically possible). This gives a total of 256 maximum possible states for the 4 bridges of a 12-pulse bipolar converter. This small number is in strong contrast with the 16.8 million combinations for all groups together.

At each time step of the transient solution, and based on the results of the previous solution step and the firing signals, the correct object is picked-up for each converter bridge. These objects are then solved together with the external power network for a *simultaneous solution* of the complete system.

The simultaneous solution of the full system prevents the accumulated phase-shift error associated with converter models in real-time simulators that use a Δt time delay to correct the separate solutions of the power network and the converter. This Δt delay technique, which is also often used to interface controllers (e.g., TACS in the EMTP) and synchronous machines to the network, can lead to instability and run-off of the solution for continuous-duty (once the simulator is turned on, it stays on) real-time power system simulators.

Another critical issue in the modelling of power electronic devices is the idealization of the current interruption process. As indicated, the converter valves are modeled as ideal conduct/block devices, which creates sustained numerical oscillations of the trapezoidal rule of integration during current interruption. These oscillations occur regardless of whether interruption takes place at an exact zero crossing of the current (thyristors) or during current chopping (GTO's).

The numerical oscillations problems can be totally eliminated using the Critical Damping Adjustment (CDA) technique of Martí-Lin [6] implemented in the Microtran program [7] and DCG/EPRI versions of the EMTP. The implementation of this technique in the developed real-time converter model resulted in the clean and accurate results shown in Figures Fig. 4 and Fig. 5.

Object-Oriented Program Design Considerations

For the test results shown in the next section, the new HVDC model was driven by a subset of OVNI, the Power System Simulator Program currently under development at UBC.

The driver subset of OVNI considers the HVDC model as an object representation of a finite state machine (FSM). That is, the model can only be in one of a finite number of states and its trajectory in the state space domain to that particular state depends on the previous state history of the model. Encapsulation allows the HVDC model-object to shield its state, and to communicate to the driver only those pieces of information needed by it to determine the model's environment variables that will induce the model to change state or not.

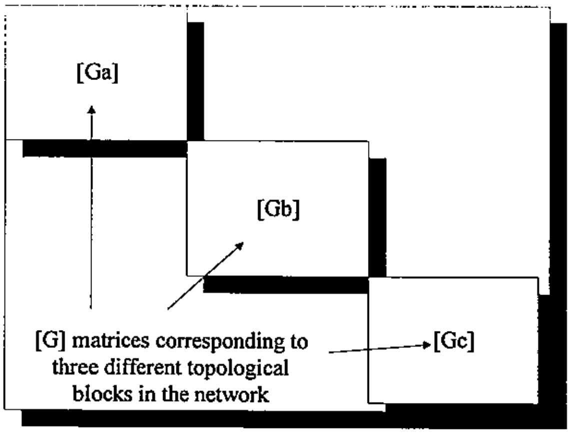


Fig. 2. Network [G] matrix for a network with topological segmentation.

OVNI, as well as its predecessor, RTNS [1], uses topological segmentation (Fig. 2) to take advantage of the network's matrix sparcity, and to allow for a convenient and efficient implementation of coarse grain parallelization.

The HVDC object model is incorporated into one of the topological blocks of Fig. 2. This scheme reduces the computational impact of state transitions in the model on the solution process for the rest of the network.

In more detail, when the HVDC object model transits to a new state, it signals the driver's corresponding block and requests a "signal-service". This service is the actualization of the subnetwork matrix to reflect the HVDC corresponding state change. Doing this at a topological block level minimizes the number of floating point operations necessary to solve the whole network in the next integration step.

III. SIMULATION RESULTS

This section presents simulation results for four case studies, as indicated in Table 1 and Fig. 3.

The system used for these tests includes a source and source impedances, the substation converter transformers, the converter bridges, and the smoothing reactors. For a full DC link, the traveling time of the transmission line divides the power system into two independent sub-areas and the task for

Table 1
Study cases

Case	Description	# of valves
1	Monopolar 6-pulse converter	6
2	Monopolar 12-pulse converter	12
3	Bipolar 6-pulse converter	12
4	Bipolar 12-pulse converter	24

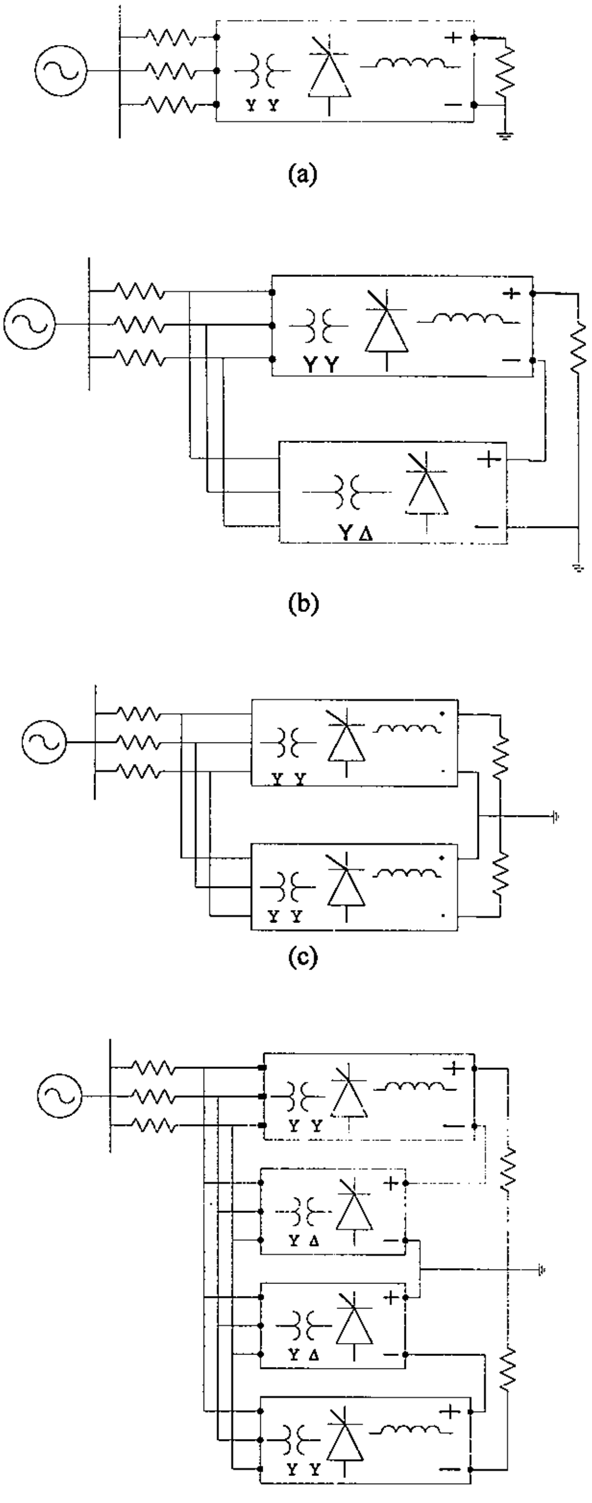


Fig. 3. Study Cases.
(a) Case 1. (b) Case 2. (c) Case 3. (d) Case 4.

Table 2
Simulation time per time-step in microseconds

Case	Microtran (v2.05-32)	RT-HVDC Simulator
1	459	26
2	983	46
3	897	51
4	3120	81

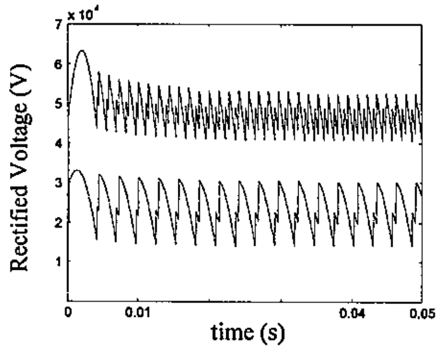
the solution of the receiving end station and associated subsystem can be given to a second processor.

Table 2 shows the simulation times obtained with the developed RT-HVDC algorithm and with the program Microtran (UBC version of the EMTP). Fig. 4 and Fig. 5 show the output plot for cases 2 and 4.

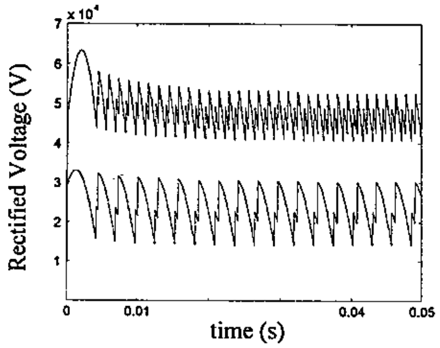
The timings indicated in Table 2 for the new algorithm and for Microtran were obtained on a Pentium Pro 200 MHz desktop computer. As indicated, the RT-HVDC algorithm is written in C++ using object-oriented program design, while Microtran is written in standard FORTRAN 77 code (it should be noted that Microtran is faster by at least a factor of two than other EMTP versions). Since the algorithm developed is to be used in a real-time simulator, the indicated simulation times correspond to the time steps requiring the largest number of operations. As can be observed from Table 2, the RT-HVDC algorithm is about 20 times faster than Microtran for the 6- and 12-pulse monopolar converters and 40 times faster for the bipolar (24-valve) converter.

The accuracy of the new algorithm was validated by comparing the simulation waveforms with those obtained with Microtran. Fig. 4 shows the rectified voltage at the first bridge and the total rectified voltage for the monopolar configuration of case 2.

Fig. 5 shows the positive and negative rectified voltages when using different firing angles in each pole for the bipolar configuration of case 4. As can be seen from these curves, the results obtained with the RT-HVDC algorithm and those obtained with Microtran are practically identical.

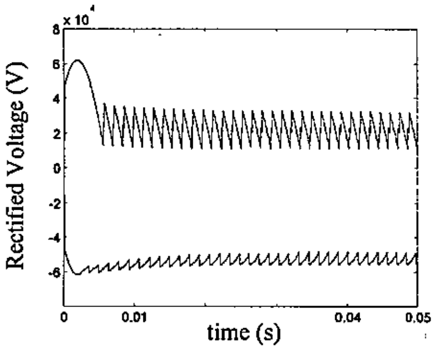


(a) RT-HVDC

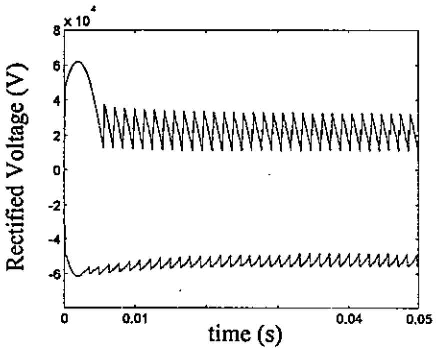


(b) Microtran®

Fig. 4. Comparison results between RT-HVDC and Microtran. Rectified voltages for Case 2.



(a) RT-HVDC



(b) Microtran®

Fig. 5. Comparison results between RT-HVDC and Microtran. Rectified voltages with different firing angles for case 4.

V. CONCLUSIONS

This paper has presented results of a common effort between The University of British Columbia, Microtran Power System Analysis Corporation, and Mitsubishi Electric Corporation to develop an efficient and accurate algorithm to represent HVDC converter stations in real-time transient simulators. The developed algorithm has minimum pre-storage requirements: only 256 matrices needed for a 24-valve station, and yet, is capable of achieving real time performance: 81 μs/step for a bipolar 12-pulse converter (24 valves), and 46 μs/step for a monopolar 12-pulse converter (12 valves) on an off-the-shelf Pentium Pro 200 MHz desktop computer.

The new real time algorithm gives numerically clean and absolutely stable results. Numerical oscillations at current interruptions are suppressed using the concepts of the CDA (critical damping adjustment) procedure of Microtran and DCG/EPRI's EMTP.

In the developed solution, the converter station model is solved simultaneously with the power system network, thus avoiding long-term instability due growing phase error in Δt-delay solution schemes. The absolute numerical stability of the algorithm makes it suitable for continuous-duty (always on) general-purpose power system simulators.

The algorithm is written in portable C++ code using object-oriented program design techniques. The algorithm makes maximum use of object decoupling techniques which account for its storage efficiency and high execution performance. This approach also allows for its easy porting to higher-performance parallel processing machines. Testing of the algorithm in high-performance parallel-processing machines is currently in progress. It is expected that the timings reported in this paper will be improved on by a factor of three or more in these machines.

V. REFERENCES

[1] Martí, J.R. and Linares, L.R., "Real-time EMTP-Based Transients Simulation", *IEEE Transactions on Power Systems*, Vol. 9, No. 3, August 1994, pp. 1304-1317.

[2] Linares, L.R. and Martí, J.R., "Sub-area latency in a real-time power network simulator", Proceeding IPST'95, International Conference on Power System Transients, Lisboa, September 1995, pp. 541-545.

[3] Kowada, Y.; Iyoda, I.; Sato, N.; Yamazaki, A.; "A study on parallel processing of electromagnetic transient simulation", IEEE Transactions on Power Systems, Vol. 10, No. 3, August 1995.

[4] Sudha, S.A.; Chandrasekaran, A.; Rajagopalan, V.; "New approach to switch modelling in the analysis of power electronic systems", *IEE Proceedings-B*, Vol. 140, No. 2, March 1993, pp. 115-123.

[5] Dommel, H.W. "EMTP Theory Book", Second Edition, Microtran Power System Analysis Corporation, Vancouver, BC, Canada, 1992.

[6] Martí, J.R. and Lin, J., "Suppression of numerical oscillations in the EMTP", *IEEE Transactions on Power Systems*, Vol. 4, No. 2, May 1989, pp. 739-747.

[7] Microtran Power System Analysis Corporation, *Microtran® Reference Manual*, Vancouver, BC, Canada, 1992.