A Predictor-Corrector Scheme for Solving a Nonlinear Circuit

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Abstract **- This paper presents a predictor-corrector iteration scheme which extends EMTP's nodal-conductance approach to include arbitrary number and configuration of nonlinear elements in a subnetwork. Because the proposed method avoids the Jacobian calculation of iteration by use of the predictor-corrector scheme, any nonlinearity can be included in a simulation by its own suitable representation. Also, the clear logic of the trivial automatic formulation of circuit equations is available in the method. Calculated results show that the method is stable for a large time step and also for simultaneous abrupt changes of the characteristics of two or more nonlinear elements.**

Keywords : nonlinear circuit, transient calculation, nodal-conductance approach, state-variable approach, predictor-corrector iteration, EMTP.

I. INTRODUCTION

For transient calculations of a power system, two major formulation approaches : 1) nodal-conductance approach (NCA) and 2) state-variable approach (SVA) were proposed. The NCA was originally proposed by H.W. Dommel [1], and the Electro-Magnetic Transients Program (EMTP) has been developed based on this approach. On the other hand, the SVA has been used in the field of electronic circuit analysis [2] and was first applied to power system transient studies by S.N. Talukdar [3].

Transient calculations of a nonlinear circuit have become more important, because modern power systems such as an HVDC (high voltage dc) system and a FACTS (flexible ac transmission system) include a number of nonlinear devices. To deal with nonlinear elements in a circuit, a compensation method was added to the NCA [4]. Although the compensation method is computationally efficient, it cannot deal with certain circuit topology such as a case that nonlinear elements create a floating subnetwork in the Thévenin equivalent calculation procedure. The compensation method usually uses the Newton-Raphson iteration to obtain the solution of a set of nonlinear circuit equations, when given nonlinear characteristics are expressed analytically, or when two or more nonlinear elements to be solved individually, even if each of them is expressed as piece-wise linear, are included in a subnetwork (disconnected by distributed-parameter lines). But the Newton-Raphson iteration requires the Jacobian of the nonlinear elements, which is sometimes difficult to be evaluated. On the other hand, the SVA is inherently able to deal with nonlinear elements, but the non-trivial automatic formulation of state equations is remained unsolved. Thus, the trivial automatic formulation of nodal equations is one of the advantages of the NCA, compared with the SVA. Sophisticated hybrid approaches combining NCA and SVA have recently been proposed [5,6].

Rather than purposing such the sophisticated approaches, this paper extends the NCA to allow an arbitrary number of nonlinear elements in a subnetwork based on a predictor-corrector iteration scheme. By extending the NCA rather than combining NCA and SVA, the clear logic of the trivial automatic formulation is available as well as the original NCA, and nonlinear elements can be connected to any branches unlike the compensation method. The present method avoids the Jacobian calculation of iteration by use of the predictor-corrector scheme. Thus, any nonlinearity can be included without evaluating its Jacobian, and each nonlinear element can be described separately in its own suitable form. Also, the method can easily be implemented in an existing EMTP-type program. Transient calculations of a single-phase diode-bridge rectifier circuit, a transistor switching circuit, and a nonlinear transformer model are demonstrated in this paper. According to the calculated results, the method is stable even for a large time step, and properly converges even when two or more nonlinear elements rapidly change their characteristics simultaneously (e.g. simultaneous switching of power devices).

II. FORMULATION OF NONLINEAR CIRCUIT

A. Optimum Ordering of Nodes

As described above, the clear logic of the trivial automatic formulation of nodal equations is one of the advantages of the NCA, and the equations of any circuit topology are expressed in the following matrix form, when all the elements in the circuit are linear :

$$\boldsymbol{G}\,\boldsymbol{v}(t) = \boldsymbol{J}(t), \tag{1}$$

where $\boldsymbol{G}$: nodal-conductance matrix, $\boldsymbol{v}(t)$: node voltage vector, and $\boldsymbol{J}(t)$: current-injection vector. Each element in the circuit is discretized by the trapezoidal rule of integration. When all the elements are linear, $\boldsymbol{G}$ remains constant and $\boldsymbol{J}(t)$ is time varying. Therefore, to save computation time, the triangular factorization of $\boldsymbol{G}$ is performed only once preceding the time-step loop, and $\boldsymbol{v}(t)$ is calculated by the backward substitution at each time step. When a circuit includes nonlinear elements, then $\boldsymbol{G}$ becomes dependent on an instantaneous solution $\boldsymbol{v}(t)$, that is, the triangular factorization of $\boldsymbol{G}$ is required during an iteration procedure at each time step. Even in this case, the computation of the triangular factorization can be minimized by ordering nodes as illustrated in Fig. 1 : from inner to outer, linear nodes without switches, linear nodes with switches, nonlinear nodes without switches, and nonlinear nodes with switches. (linear node : only linear elements are connected, nonlinear node : one or more nonlinear elements are connected.) At each time step, only the portion of the nonlinear nodes is factorized during an iteration procedure. When one or more switches operate, then the portion of the linear nodes with switches is also factorized. The portion of the linear nodes without switches remains unchanged through out a simulation. This ordering approach is closely related to one proposed for the compensation method in [4].

B. Predictor-Corrector Iteration

When a target circuit includes nonlinear elements, G becomes dependent on an instantaneous solution $v(t)$, and an iteration procedure is required to find the solution of the following nodal-conductance equation :

$$G(t, v(t))\, v(t) = J(t). \tag{2}$$

The present method uses a predictor-corrector scheme for the iteration, because it does not require the Jacobian, which is sometimes difficult to be evaluated. The solution of the following equation $v^{(0)}(t)$ gives the first estimation of the iteration (= predictor) :

$$G(t, v(t-\Delta t))\, v^{(0)}(t) = J(t). \tag{3}$$

It should be noted that $v^{(0)}(t)$ is different from the solution at the previous time step, because J(t) has already been updated in (3). Then, improved solutions are recursively obtained by the following iteration scheme (= corrector) :

$$G(t, v^{(k-1)}(t))\, v^{(k)}(t) = J(t), \tag{4}$$

where k = 1, 2, ⋯ is the number of iteration. When the maximum difference of an improved solution from the previous iteration step becomes smaller than a user specified error constant ε, namely,

$$\max_i \left|\Delta v_i^{(k)}\right| = \max_i \left|v_i^{(k)} - v_i^{(k-1)}\right| < \varepsilon \quad (i : \text{node index}), \tag{5}$$

then $v^{(k)}(t)$ is regarded as the solution, and we now proceed to the next time step. It should be noted that the proposed scheme requires no restriction on the number and configuration of nonlinear nodes, and thus arbitrary number of nonlinear elements can be connected to any branches. Also, because the proposed scheme does not modify the basic equation of the NCA, the trivial automatic formulation of (2) is still available as well as the original NCA. Those features facilitate the implementation of the proposed scheme in an existing EMTP-type program. Any integration rule can be used to discretize each element, but the trapezoidal rule may be preferred in terms of accuracy, speed, and stability.

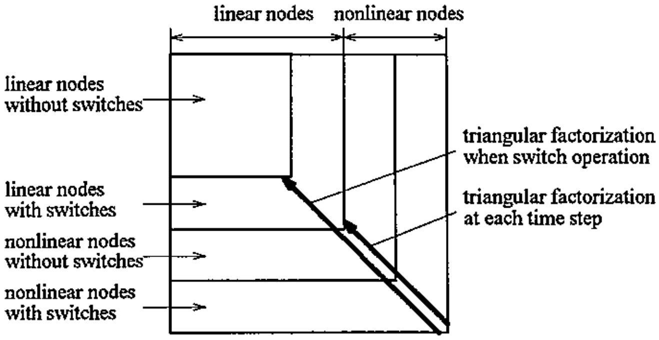


Fig. 1 Nodal-conductance matrix G

C. Relation with ODE Formulation

The predictor-corrector scheme described above starts an iteration with a solution predicted from the information available at the previous time step, and then simply improves the predicted solution recursively. The scheme seems different from the standard predictor-corrector scheme of ordinary differential equations (ODEs) [2]. But it can be shown that the present scheme is mathematically the same as the standard scheme as follows. Consider a set of nonlinear ODEs (state equations) describing the dynamics of a circuit :

$$\frac{dx(t)}{dt} = f(x(t), u(t), t) \tag{6}$$

where $x(t)$: state-variable vector and $u(t)$: input vector. Applying the trapezoidal rule of integration, we obtain the following implicit formula :

$$x(t) = x(t-\Delta t) + \frac{\Delta t}{2}\{f(x(t-\Delta t), u(t-\Delta t), t-\Delta t) + f(x(t), u(t), t)\}. \tag{7}$$

The standard predictor-corrector scheme modifies the above into the following recursive formula :

$$x^{(k)}(t) = x(t-\Delta t) + \frac{\Delta t}{2}\{f(x(t-\Delta t), u(t-\Delta t), t-\Delta t) + f(x^{(k-1)}(t), u(t), t)\}, \tag{8}$$

where k = 1, 2, ⋯ is the number of iteration. Because the above formula can not start by itself, the forward Euler rule :

$$x^{(0)}(t) = x(t-\Delta t) + \Delta t f(x(t-\Delta t), u(t-\Delta t), t-\Delta t) \tag{9}$$

is usually used to obtain the initial guess of the iteration. Equation (9) predicts the present solution only from the information available at the previous time step, and thus called a predictor. Then, (8) recursively improves the predicted solution, and thus a corrector. On the other hand, (3) predicts the present solution, and (4) recursively improves the predicted solution, in the same manner as (9) and (8) respectively. Therefore, the proposed scheme can be regarded as an NCA version of the predictor-corrector method.

D. Comparison with Compensation Method

In the compensation method, we first have to build the Thévenin equivalent of the linear portion of a circuit seen from nonlinear branches. The voltage source of the Thévenin equivalent is calculated by replacing the nonlinear branches with open-circuit branches. Consider an example circuit illustrated in Fig. 2(a). When the Thévenin equivalent of the circuit is calculated, the nonlinear elements are disconnected as shown in Fig. 2(b), and a floating subnetwork is created. The voltages of node **N1** and **N2** cannot be calculated. Fig. 2(c) illustrates another example. When both the nonlinear inductance and resistance are disconnected, the voltage of node **N2** becomes unknown as shown in Fig. 2(d). In the former case, a large resistance may be put in parallel with each nonlinear element, but this slightly modifies the solution. In the latter case, if both the nonlinear elements are modeled as one element, then the voltage of node **N2** is not necessary to be calculated. But this considerably reduces the maintainability of each model in terms of the modularity of a model. On the other hand, the proposed method can deal with those cases without any modification. Each model can be developed independently, and a model can easily be used for other purposes. Also, the avoidance of the Jacobian calculation enhances the general describability of a model. Therefore, the proposed method may show a good performance together with a model description language such as the MODELS language [7].

E. Modeling of Nonlinear Component

The characteristics of a nonlinear element may be described using a language such as Fortran, C, or MODELS, or may be given as a point list representing its piece-wise linear characteristics. Whatever description method is used, it is quite important to make clear the types of information to be exchanged between a host program which performs the present predictor-corrector scheme and a model describing a nonlinear element. The host program first gives a predicted branch voltage $v_b^{(0)}$ obtained by (3) to the model. The model calculates the equivalent conductance $G_{eq}^{(1)}$ and current source $J_{eq}^{(1)}$ from the predicted branch voltage, and gives them back to the host program. Then, the host program starts an iteration based on (4). During the iteration, the host program gives an improved branch voltage $v_b^{(k)}$, and the model gives back the conductance $G_{eq}^{(k+1)}$ and current source $J_{eq}^{(k+1)}$ for the next iteration step in the same manner. A certain nonlinearity requires to be expressed as a function of its branch current instead of voltage. In this case, the branch current $i_b^{(k)}$ is calculated from the given branch voltage $v_b^{(k)}$ as :

$$i_b^{(k)} = G_{eq}^{(k)} v_b^{(k)} + J_{eq}^{(k)}, \tag{10}$$

and then used in order to calculate $G_{eq}^{(k+1)}$ and $J_{eq}^{(k+1)}$. Especially as for the v - i characteristic of a switching device, the equivalent conductance should be calculated as a function of v where $\partial i/\partial v$ is gentle, and a function of i where $\partial i/\partial v$ is steep, for the stable convergence of iteration.

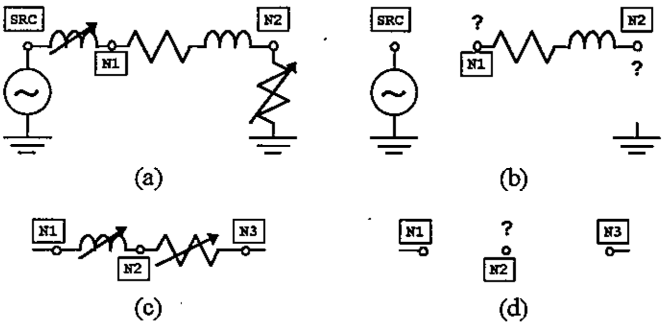


Fig. 2 Problems of the compensation method

III. EXAMPLES

A. Single-Phase Diode-Bridge Rectifier Circuit

A single-phase diode-bridge rectifier circuit illustrated in Fig. 3 is analyzed using the proposed method. Each diode in the circuit is modeled as a nonlinear resistance of which the v - i characteristic is defined in Fig. 4. Measured v - i characteristic is approximated by $v(i) = 81.65\times10^{-3} \ln (51.03 \times 10^{6}\, i)$, and its equivalent resistance R_D is calculated as :

$$R_D = v(i)\,/\,i \quad (V > 0), \quad R_D = 400\ \text{k}\Omega \quad (V \le 0). \tag{11}$$

Because $\partial i/\partial v$ is considerably steep when the diode is on, the equivalent resistance is calculated as a function of i. A startup transient is calculated, and node voltage waveforms are shown in Fig. 5. For this simulation, Δt = 0.1 ms (166.7 points / period) may be reasonable and the calculated waveforms are plotted using solid lines. Even when Δt is set to 2.0 ms (8.3 points / period), the calculated results are still stable and plotted using

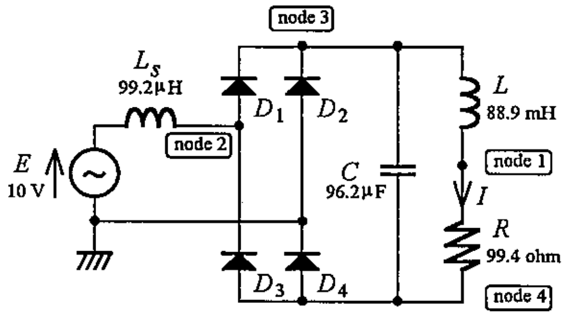


Fig. 3 Single-phase diode-bridge rectifier circuit

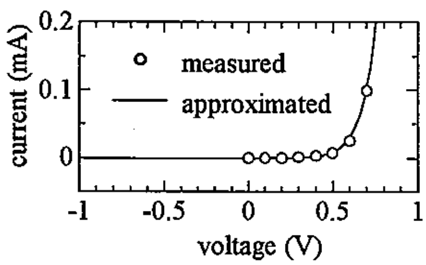


Fig. 4 Voltage-current (v - i) characteristic of diode

broken lines. It is clear that the present method is stable even for a large time step. The calculated waveforms of the input voltage and the output current are replotted in Fig. 6(a), and agree well with measured ones shown in Fig. 6(b).

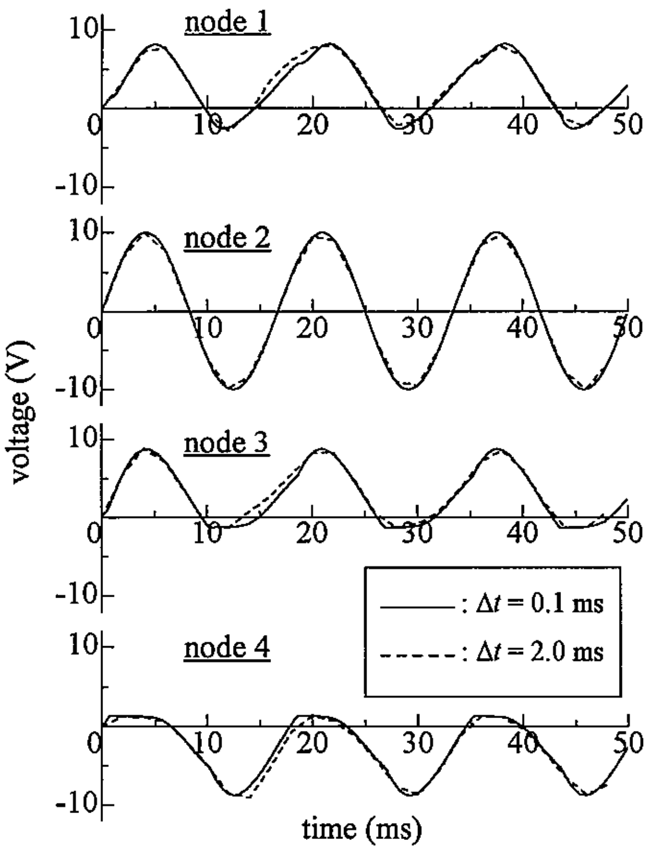
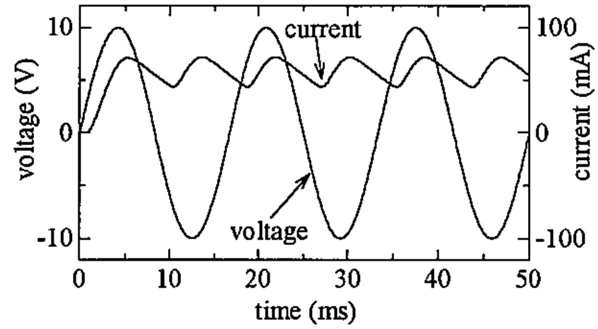


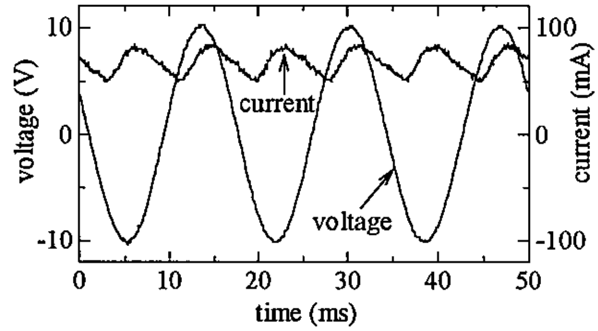
Fig. 5 Calculated waveforms of node voltages

B. Transistor Switching Circuit

An inverter-type transistor switching circuit is illustrated in Fig. 7. The circuit includes four transistors and four diodes, thus eight nonlinear elements. Each transistor is modeled as a nonlinear resistance, and the v - i characteristic (V_{CE} : collector-emitter voltage versus I_C : collector current, with parameter I_b : base current) is given in Fig. 8. On and off delays, and rising and falling time constants are considered in the transistor model [8]. The diodes are modeled in the same manner as in the previous example. Fig. 9(a) shows base-current waveforms controlling the transistors. I_{b1} controls Tr1 and Tr4, and I_{b2} Tr2 and Tr3. The voltage waveform across the load is calculated by the proposed method and shown in Fig. 9(b). The calculated result agrees well with measured one shown in Fig. 9(c). Although eight nonlinear elements abruptly change their characteristics simultaneously, the proposed predictor-corrector scheme properly converges.



(a) calculated (startup)



(b) measured (steady state)

Fig. 6 Measured waveforms of input voltage and output current

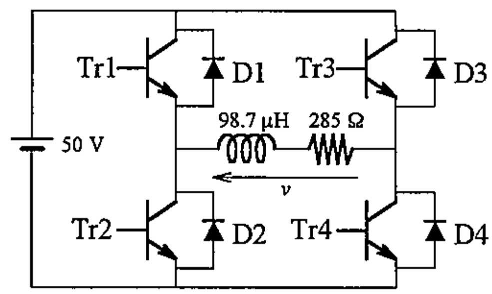


Fig. 7 Inverter-type transistor switching circuit

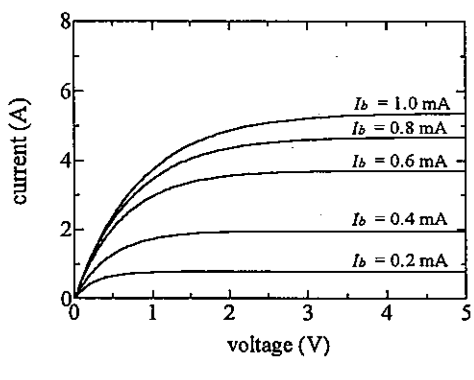
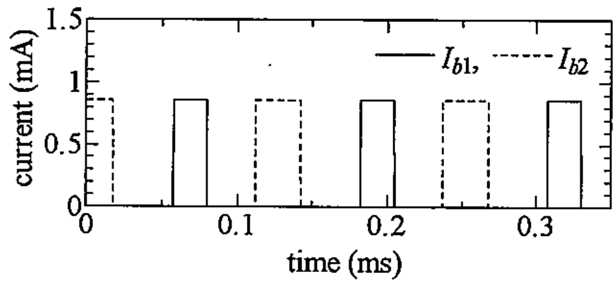
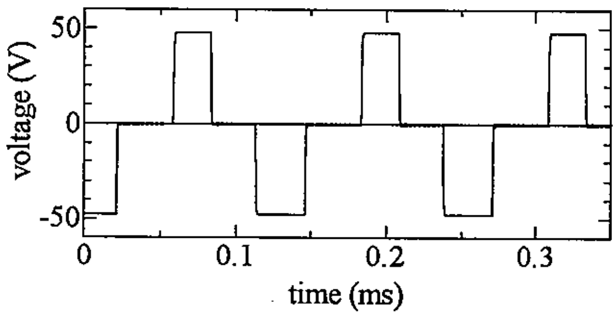


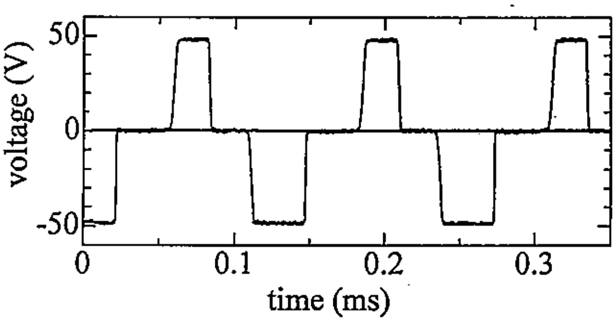
Fig. 8 V_{CE} - I_C characteristic of a transistor



(a) base current



(b) calculated voltage waveform across load



(c) measured voltage waveform across load

Fig. 9 Simulation of transistor switching circuit

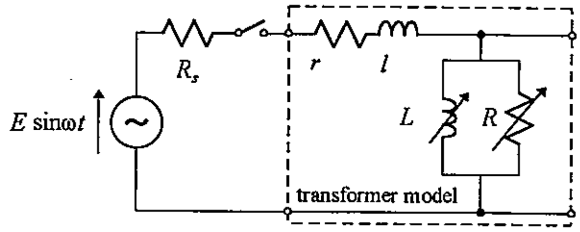
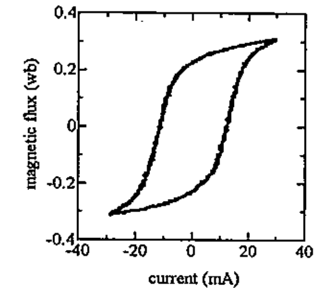
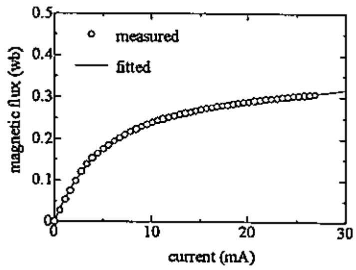


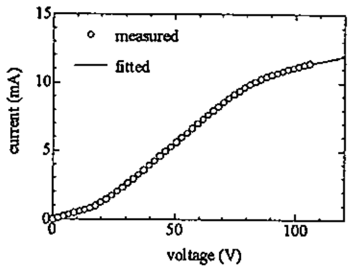
Fig. 10 Transformer model



(a) hysteresis curve



(b) i - ϕ characteristic



(c) v - i characteristic

Fig. 11 Iron-core nonlinearity of transformer

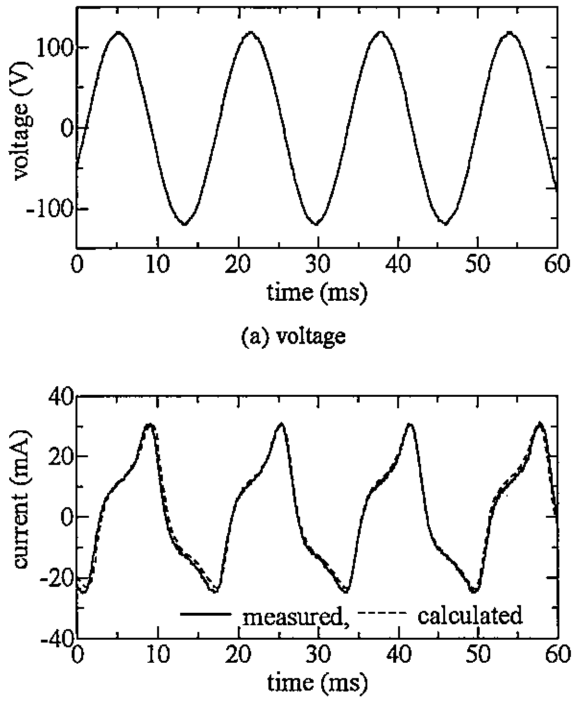
C. Transformer Model

The iron-core nonlinearity of a transformer has to be included in a simulation predicting harmonics and inrush currents. A transformer model proposed by L.O. Chua et. al. [9] is illustrated in Fig. 10. The iron-core nonlinearity is modeled by a nonlinear inductance and resistance connected in parallel. Fig. 11(a) shows a measured hysteresis loop of an 100-V transformer. From the hysteresis loop, the nonlinearities of the inductance and resistance are determined as proposed in [9] and shown in Fig. 11(b) and (c) respectively. Each of the determined nonlinearities is then approximated by a polynomial, and used in the subsequent simulations. The winding resistance and the leakage inductance were measured to be 22.9 Ω and 5.79 mH in the primary side. Fig. 12(a) shows a measured applied-voltage waveform, and Fig. 12(b) shows measured and calculated current waveforms. Those current waveforms show a good agreement. The calculated result is obtained by the proposed method running a simulation until the calculated waveform is settled in a steady-state. A startup transient is also calculated and shown in Fig. 13. Inrush currents are reproduced by the simulation.

The measured waveforms in Figs. 6(b), 9(c), and 12(b) were obtained by assembling actual circuits of Figs. 3, 7, and 10 respectively, and recorded using a digitizing oscilloscope.

D. Computational Efficiency and Accuracy

In order to demonstrate the computational efficiency of the proposed transient calculation method, the computation times of the above three examples with and without the predictor-corrector (PC) scheme are given in Table 1. In those calculations, the error constant of (5) was set to 1.0×10^{-6}, and an 133 MHz Pentium-based computer was used under Win95. It should be noted that the PC scheme requires a small amount of extra computation time. To show the accuracy of the proposed method, the same startup transient as Sec. III-A is calculated with and without the PC scheme. The calculated waveforms of the output current I are shown in Fig. 14. It is clear that the PC scheme significantly improves the accuracy. Without the PC scheme, the calculated waveform is different from measured one shown in Fig. 6(b), and numerical oscillations are also observed. This is due to inaccurate switching timings of the diodes, because the on/off state of a diode is determined by the information at the previous time step (like the use of TACS in EMTP). Therefore, the proposed PC scheme requires a small amount of extra computation time but significantly improves accuracy.



(a) voltage

(b) current

Fig. 12 Voltage and current waveforms of transformer

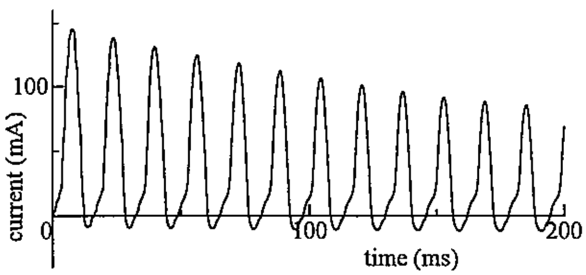


Fig. 13 Startup transient of transformer

Table 1 Comparison of computation time

*	Δt	T_{max}	with PC	without PC	ratio
A	0.1 ms	50 ms	1.59 s	0.77 s	2.06
B	0.2 μs	500 μs	5.82 s	5.33 s	1.09
C	0.3 ms	300 ms	2.31 s	2.09 s	1.11

(*) A: diode-bridge rectifier circuit, B: inverter circuit, C: transformer model

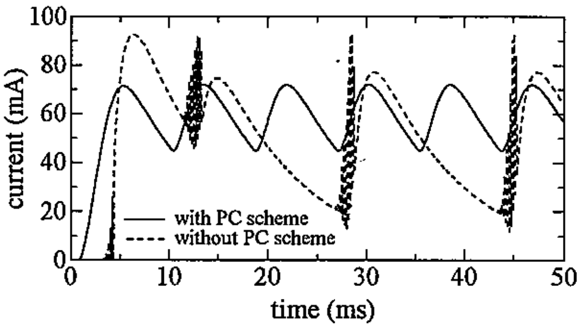


Fig. 14 Comparison of accuracy

IV. CONCLUSIONS

An extension to the NCA has been presented to allow arbitrary number and configuration of nonlinear elements in a subnetwork by use of the predictor-corrector scheme. The trivial automatic formulation is available in the method as well as the original NCA, and nonlinear elements can be connected to any branches unlike the compensation method. The method avoids the Jacobian calculation of iteration which is sometimes difficult to be evaluated. The present method has been applied to a single-phase diode-bridge rectifier circuit, a transistor switching circuit, and a nonlinear transformer model, and the calculated results agree well with actual measurements. The proposed scheme has shown to be robust even for a large time step, and also for simultaneous and abrupt changes of the characteristics of nonlinear elements.

REFERENCES

[1] H.W. Dommel, "Digital computer solution of electromagnetic transients in single- and multi-phase networks," *IEEE Trans.*, Power App. and Syst., Vol. PAS-88 (4), pp. 388-398, 1969

[2] R.A. Rohrer, "Circuit Theory: An introduction to the state-variable approach," McGraw-Hill, 1971.

[3] S.N. Talukdar, "METAP - A modular and expandable program for simulating power system transients," *IEEE Trans.*, Power Apparatus and Systems, Vol. PAS-95 (6), pp. 1882-1891, 1976.

[4] H.W. Dommel, "Nonlinear and time-varying elements in digital simulation of electromagnetic transients," *IEEE Trans.*, Power Apparatus and Systems, Vol. PAS-90, pp. 2561-2567, 1971.

[5] J.M. Zavahir, J. Arrillaga, and N.R. Watson, "Hybrid electromagnetic transient simulation with the state variable representation of HVDC converter plant," *IEEE Trans.*, Power Delivery, Vol. PWRD-8 (3), pp. 1591-1598, 1993.

[6] Y. Kang and J.D. Lavers, "Transient analysis of electronic power systems: reformulation and theoretical basis," *IEEE PES Summer Meeting*, 95 SM 518-1 PWRS, 1995.

[7] L. Dubé and I. Bonfanti, "MODELS: A new simulation tool in the EMTP", *European Trans. on Electrical Power Engineering* (ETEP), Vol.2, no.1, pp.45-50, January/February 1992.

[8] N. Nagaoka, S. Fujii, and A. Ametani, "An analysis of operational characteristics of high frequency inverters by EMTP," *PESC '88* Record, pp. 731-738, 1988.

[9] L.O. Chua and K.A. Stromsmoe, "Lumped-circuit models for nonlinear inductors exhibiting hysteresis loop," *IEEE Trans.*, Circuit Theory, Vol. CT-17, No. 4, 1970.